TECHNISCHE UNIVERSITÄT DRESDEN

NEW GATE DRIVE UNIT CONCEPTS FOR IGBTS AND REVERSE CONDUCTING IGBTS

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New Gate Drive Unit concepts for IGBTs and Reverse Conducting IGBTs

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NOMENCLATURE

α_{pnp}	Current gain of the pnp-transistor
C	DC-link capacitance
C_{CE}	IGBT's internal collector-emitter capacitance
C_{GC}	IGBT's internal gate-collector capacitance
C_{GE}	IGBT's internal gate-emitter capacitance
c_S	Control signal for the controlled DC-DC converter
D	Diode symbol in equivalent circuits
D_C	Duty cycle
$\overline{d_{Cm}}$	Acquired value to estimate the collector current from the current estimation methods
di/dt	Current change ratio
dv/dt	Voltage change ratio
E_{sw}	Switching losses
E_R	Current estimation error, for the current estimation methods
E	Electric field strength
f_c	Cut-off frequency
f_{sw}	Switching frequency
g_{fs}	Forward transconductance
i_C	Collector current (time dependent)
I_C	Collector current
$\widehat{I_{C,cal}}$	Maximal collector current for the calibration of the current estimation methods
i_{CG}	Collector-gate current of the IGBT (time dependent)
$\overline{i_{Cm}}$	Estimated current from the current estimation methods
I_{CN}	Nominal collector current
$i_{C,RC}$	RC-IGBT current when it acts as an IGBT (time dependent)
$I_{C,sat}$	Saturation current of IGBT
$I_{C,SCI}$	Peak collector current during a short circuit type I
$I_{C,SCII}$	Peak collector current during a short circuit type II
i_D	Diode current (time dependent)
$i_{D,RC}$	RC-IGBT current when it acts as a diode (time dependent)
$I_{D,RC}$	RC-IGBT current when it acts as a diode
i_G	Gate current of the IGBT (time dependent)
i_L	Load current (time dependent)
I_L	Load current
i_{RRM}	Diode reverse recovery current (time dependent)
$i_{RR,D,RC}$	Reverse recovery current of the RC-IGBT in the diode mode (time dependent)
$I_{RR,D,RC}$	Peak reverse recovery current of the RC-IGBT in the diode mode

$i_{int,i}$	Output signal of the current estimation method by integration
i_S	Current through the switch device (time dependent)
$i_{S,RC}$	Current through of the RC-IGBT (time dependent)
κ	Channel conductivity
k_{SC1}	Counter used for the detection of a SCI in the FSCP scheme
k_{SC2}	Counter used for the detection of a SCII in the FSCP scheme
L_{bond}	Internal stray inductance of the connection between auxiliary and power emitter in a semiconductor device module
L_{Load}	Load inductor
L_σ	Stray inductance
m_a	Modulation index
n	Electron density
p	Hole density
P_{CON}	Conduction power losses
φ	Phase angle between the fundamental components of voltage and current
P_{OFF}	Turn-off power losses
P_{ON}	Turn-on power losses
R_B	Base resistance of a BJT
r_{SC1}	Reference limit value used for the detection of a SCI in the FSCP scheme
r_{SC2}	Reference limit value used for the detection of a SCII in the FSCP scheme
R_D	Drift resistance in the IGBT chip structure
R_G	External gate resistance
$R_{G,int}$	Internal gate resistance of the semiconductor device
$R_{G,OFF,D}$	Gate turn-off resistance of the RC-IGBT in the diode mode
$R_{G,OFF}$	Gate turn-off resistance
$R_{G,ON}$	Gate turn-on resistance
$R_{G,tot}$	Total gate resistance ($R_{G,int} + R_G$)
R_W	Lateral p-well resistance in the IGBT chip structure
s	Digital command signal of the semiconductor device
$SCIs$	Digital signal that shows if a SCI has been produced (used for the FSCP scheme)
$SCIIs$	Digital signal that shows if a SCII has been produced (used for the FSCP scheme)
T	Semiconductor device symbol in the equivalent circuits
t	Time
t_d	Delay time
$t_{d,opt}$	Optimal delay time
$t_{GC,RC}$	Instant time of the MOS-channel closing ($V_{GE,RC} < V_{GE,th,RC}$)
T_j	Junction temperature
T_{jmax}	Maximum junction temperature
$t_{meas,i\text{-}off}$	Period of time that $v_{meas,i\text{-}off}$ signal is high (used to estimate the current)
$t_{meas,i\text{-}on}$	Period of time that $v_{meas,i\text{-}on}$ signal is high (used to estimate the current)
t_{PT}	Length of the PT pulse
t_{zc}	Time instant of the RC-IGBT zero crossing current
v_{bond}	Voltage across the internal stray inductance L_{bond} (time dependent)
V_{BR}	Breakdown voltage
v_{CC}	DC-link voltage (time dependent)
V_{CC}	DC-link voltage
v_{CE}	Collector-emitter voltage (time dependent)
V_{CE}	Nominal collector-emitter voltage
$V_{CEm,sat}$	Measured voltage of the collector-emitter saturation voltage of the RC-IGBT
$v_{CE,RC}$	RC-IGBT collector-emitter voltage (time dependent)
$V_{CE,sat}$	Collector-emitter saturation voltage
$v_{cmp,sat}$	Signal used to determine the state of the RC-IGBT (IGBT or diode)
v_D	Diode's anode-cathode voltage (time dependent)
V_D	Diode's anode-cathode voltage
v_f	Diode's forward voltage (time dependent)
V_f	Diode's forward voltage
v_{GE}	Gate-emitter voltage (time dependent)

V_{GEoff}	Gate-emitter turn-off voltage
V_{GEon}	Gate-emitter turn-on voltage
$v_{GE,RC}$	Gate-emitter voltage of the RC-IGBT (time dependent)
$v_{meas,i\text{-}off}$	Output signal of the current estimation method by comparison during the turn-off transient
$v_{meas,i\text{-}on}$	Output signal of the current estimation method by comparison during the turn-on transient
V_m	Miller effect voltage
V_n	GDU negative power supply voltage
V_p	GDU postive power supply voltage
V_{ref}	Reference voltage
$V_{ref\text{-}off}$	Reference voltage for the current estimation method by comparison during the turn-off transient
$V_{ref\text{-}on}$	Reference voltage for the current estimation method by comparison during the turn-on transient
$V_{GE,th}$	Gate-emitter threshold voltage
$V_{GE,th,RC}$	Gate-emitter threshold voltage of the RC-IGBT
w_B	Width of the drift layer, middle region in a semiconductor device
W_{OFF}	Turn-off energy losses of the semiconductor device
$W_{OFF,D}$	Turn-on energy losses of a Diode
$W_{OFF,D,RC}$	Turn-off energy losses of the RC-IGBT operated in the diode mode
W_{ON}	Turn-on energy losses of the semiconductor device
W_{TOT}	Total energy switching losses $W_{TOT} = W_{ON} + W_{OFF} + W_{OFF,D}$

ACRONYMS

2L-VSC	two level voltage-source converter
ADC	analog-to-digital converter
BIGT	bi-mode insulated-gate transistor
BJT	bipolar junction transistor
cat 5e	twisted pair cable category 5 enhanced
CEC	current estimation by comparison
CEI	current estimation by integration
CS	current source
DAC	digital-to-analog converter
DTC	direct torque control
DUT	device under test
EMI	electromagnetic interference
FPGA	field-programmable gate array
FSCP	fast short circuit protection method
GDU	gate drive unit
GTO	gate turn-off thyristor
I^2t-value	Ampere squared seconds
IC	integrated circuit
IGBT	insulated-gate bipolar transistor
IGBT4	fourth generation IGBT
IGCT	integrated-gate commutated thyristor
LV	low voltage
MOSFET	metal-oxide-semiconductor field-effect transistor
MV	medium voltage
NPT-IGBT	non-punch-through IGBT
NTC	negative temperature coefficient
PCB	printed circuit board
PP	press-pack
PT	pre-trigger
PTC	positive temperature coefficient
PT-IGBT	punch-through IGBT
PWM	pulse width modulation
RBSOA	reverse bias safe operation area
RC-IGBT	reverse conducting IGBT
RRSOA	reverse recovery safe operation area
SCI	short circuit type 1
SCII	short circuit type 2
SCSOA	short circuit safe operation area

Si	silicon
SiO_2	silicon dioxide
SLR	switching loss reduction scheme
SOA	safe operation area
SPT-IGBT	soft punch through IGBT
VS	voltage source
VSC	voltage-source converter

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1 INTRODUCTION

Power electronics systems and power converters have been an indispensable element in the development of e.g. mining, marine and energy generation branches. Nowadays, they cover industrial applications such as fans, pumps, compressors in the mining, chemical, oil and gas industry, among others. These systems convert, regulate and optimize the use of electric power with high efficiency and reliability. Power semiconductor devices are an essential component of converters influencing their power range, efficiency, volume and cost. Presently, the insulated-gate bipolar transistor (IGBT) is one of the most used semiconductor devices in medium voltage (MV) converters, due to its low conduction losses, controllable turn-on and turn-off transients and its capability to endure short circuits for a certain period of time.

An IGBT is driven by an electronic circuit called a gate drive unit (GDU) or gate unit, which provides an interface between the upper or central control unit and the semiconductor device. Presently, GDU does not only trigger the IGBT to switch on or off, but also protects it against short circuits and over-voltages. Thus, a high reliability and availability of the power converter system can be achieved. More advanced GDUs, also called intelligent GDUs, can regulate the collector current and/or the collector-emitter voltage during the turn-on and turn-off transient of the IGBT and thus the switching behaviour can be improved. The disadvantages of these intelligent GDUs are their expensive electronic realization, such as: incorporation of a micro controller or FPGA, measurement of the collector current trough Rogowski or Hall sensors, fast analog-to-digital converters, etc.

The work presented in this doctoral thesis is focused on the concept development of novel GDU schemes for different tasks. Although the main focus of this work are 1200 V and 1700 V IGBTs, the concepts, principles and results can be transferred also to other IGBT voltage classes. Exemplarily two novel schemes are introduced to estimate the collector current through the IGBT. These schemes are based on the measurement of the voltage across the internal stray inductance of the IGBT module. Furthermore, a concept was derived to balance the on-state collector currents of parallel-connected IGBTs, where the gate-emitter voltage is actively modified, according to the estimated value of the collector currents.

Continuing, a new scheme for fast short circuit protection is proposed that combines a fast short circuit detection and a safe turn-off procedure. The improvements of IGBT turn-on and turn-off transients by improved gate unit switching profile as well as the conduction of IGBTs as increased gate-emitter voltages will be considered.

Moreover, the switching behaviour of a new IGBT structure named as reverse conducting IGBT (RC-IGBT) is investigated. This device integrates an IGBT and an anti-parallel diode into one single

chip. Therefore, RC-IGBTs can operate as an IGBT or as a diode, providing high power density and advantages regarding thermal cycling.

The proposed concepts have been experimentally tested with IGBT modules and implemented with a simple and inexpensive electronic circuitry, which is an important feature for possible industrial implementations. During the course of this work, two papers were presented [1, 2] and three patent applications were filed [3–5].

This thesis begins with an overview of IGBTs and conventional GDU schemes, considering typical protection schemes against short circuits and over-voltages. In chapter three, new current estimation methods are described. The fourth chapter presents the investigation of RC-IGBTs. The static balancing of IGBTs connected in parallel, fast short circuit protection schemes, and the operation of IGBTs with a higher gate-emitter voltage are presented in the fifth chapter. Finally, the chapter six presents the conclusions of this work.

2 STRUCTURE, FUNCTION AND APPLICATIONS OF IGBTS

An ideal switching device should have low (ideally zero) conduction and switching losses. Besides, it should have a high power density and controllable turn-on and turn-off transients. Since the discovery of the pn junction, different power semiconductors have been developed seeking to approach the characteristics of an ideal switch.

Traditional power switching devices are based on transistor and thyristor structures. The thyristor is the best option in applications where the control of device turn-off is not needed. When the point in time of a turn-off transient of the device must be adjusted, semiconductor devices such as the gate turn-off thyristor (GTO) or the integrated-gate commutated thyristor (IGCT) can be used. These devices offer a high power density. However, they require a high gate drive power to be triggered. Besides, the switching transient can not be controlled. Therefore a clamping circuit and a snubber must be included to limit the rate of change of the current and voltage, *di/dt* and *dv/dt* [6–8].

Semiconductor structures based on transistors can be either unipolar or bipolar, depending on the charge carrier type (holes or electrons, or a combination of both). Bipolar junction transistors (BJTs) are used for low voltage (LV) applications. Unfortunately, BJTs have low current amplification, low blocking capability and require a constant base current during conduction [6, 7].

To overcome the BJT's problems, a semiconductor device called metal-oxide-semiconductor field-effect transistor (MOSFET) was developed. This device features high current capability, fast turn-on and turn-off transients, low switching losses and a high input impedance, which leads to a low driving power. However, high voltage MOSFETs (>600 V) present high conduction losses at high current densities, due to its unipolar structure.

During the continuous development towards the ideal power switching device, new semiconductor devices called insulated-gate bipolar transistors (IGBTs) [9] were developed and introduced in the market at the beginning of the 1980s [10]. These devices overcome the disadvantages previously mentioned by combining the characteristics of BJTs and MOSFETs.

Nowadays, IGBTs dominate the device market between 1200 V and 3300 V. Over 3300 V, the IGBT and the IGCT share the market [7]. Nevertheless, the constant improvements of IGBTs make these devices more and more attractive in high power applications. This chapter gives an overview of these type of devices. Moreover, the basic circuits to trigger and protect them are presented.

Currently, modified IGBT structures named reverse conducting IGBTs (RC-IGBTs) are being developed. These devices have a high power density and advantages in thermal cycling [11], due to the inclusion of a diode in the IGBT die [6, 12]. This topic is discussed in Chapter 4.

2.1 STRUCTURE AND OPERATION OF THE IGBT

The basic IGBT structure is similar to that of a vertical power MOSFET. The difference between these two devices, as shown in Fig. 2.1, is that the n-doped layer in the drain region of the MOSFET is replaced by a p^+ layer in the IGBT. This IGBT chip structure, known as non-punch-through IGBT (NPT-IGBT), was the first one to be developed [6, 7, 9]. The main terminal at the bottom p^+ layer is named collector terminal and at the top the n^+ layer is referred to as emitter. The gate terminal is isolated from the body by a silicon dioxide (SiO_2) layer. Details of IGBT and MOSFET structures are presented in [6–9].

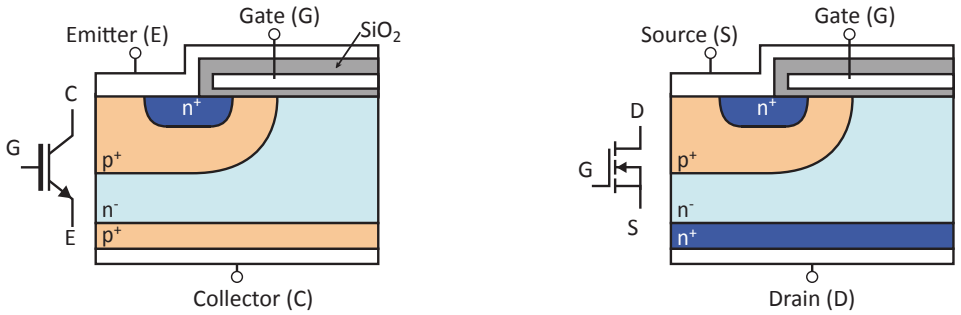


Figure 2.1: Chip structure and symbol [6–8]. (a) IGBT (NPT chip structure), and (b) N-channel MOSFET (vertical chip structure).

An equivalent circuit of the IGBT is presented in Fig. 2.2, where $R_{G,int}$ is the internal gate resistance, R_D is the drift resistance, R_W is the lateral p-well resistance, C_{GE} is the internal gate-emitter capacitance, C_{GC} is the internal gate-collector capacitance and C_{CE} is the internal collector-emitter capacitance [10]. The drain of the MOSFET T_3 is connected to the base of the pnp-transistor T_1 through R_D. The parasitic npn-transistor T_2 together with T_1 form a parasitic thyristor. Under certain conditions, e.g. very high current, T_2 can be turned on. As a result, the parasitic thyristor latches up and the collector current i_C increases uncontrollably, leading to the destruction of the IGBT.

The principle of operation of the IGBT is explained on the basis of Fig. 2.3. A positive collector-emitter voltage ($v_{CE} > 0\,V$) and a gate-emitter voltage larger than the threshold voltage ($v_{GE} > V_{GE,th}$) are applied. As a consequence, a MOS channel is formed between n^+ and n^- layer represented by T_3 and electrons flow from the emitter into the n^- region, which is the base of the pnp-transitor T_1. The pn junction of the collector side is forward biased and holes are injected into the n^- region. Thus, its resistance is reduced and the carrier density as well as the current are increased [6, 13].

If v_{GE} is lower than the threshold voltage ($v_{GE} < V_{GE,th}$), the MOS channel is suppressed and the collector pn junction of T_1 is reverse biased. The excess holes are absorbed by recombination, which generate the tail current, a typical feature of bipolar devices.

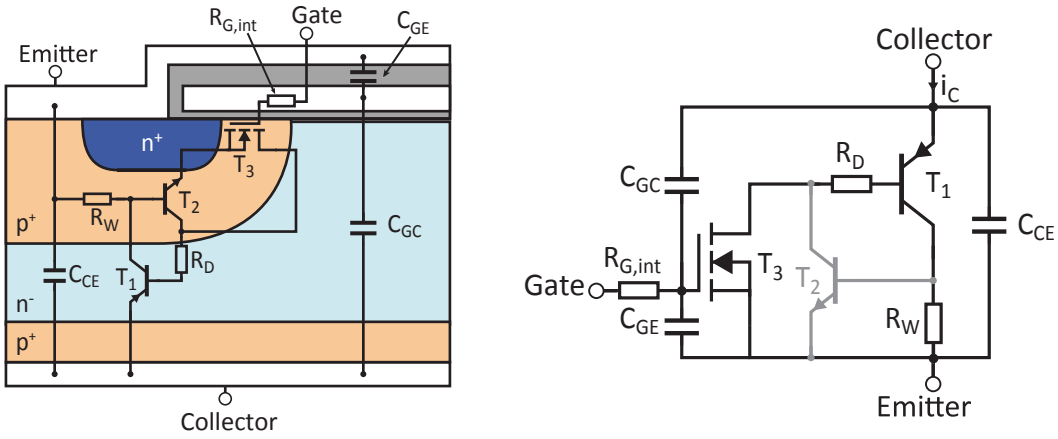


Figure 2.2: IGBT representation [6, 7, 10]. (a) Chip structure, and (b) equivalent circuit.

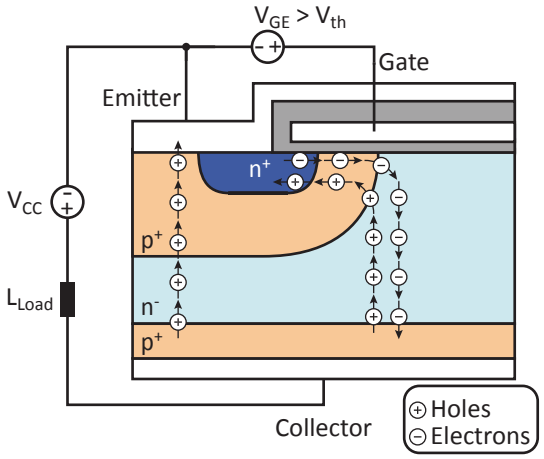


Figure 2.3: Representation of the carrier flow in an IGBT [6, 7, 10].

The NPT-IGBT structure features a triangular electric field shape, as presented in Fig. 2.4. This chip structure improves the robustness against latch-up and it also can withstand short circuit, due to the wider base w_B and lower gain of the pnp-transistor [14]. Moreover, this structure provides a positive temperature coefficient (PTC), which is favourable for parallel connection of IGBTs.

NPT-IGBTs are produced with an ion implantation technology [6, 15]. This process allows an accurate adjustment of the emitter efficiency.

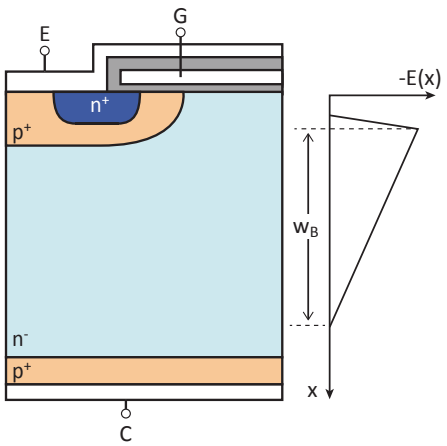


Figure 2.4: Representation of an NPT-IGBT chip structure [6, 14, 15].

An alternative to NPT-IGBT is the punch-through IGBT (PT-IGBT) structure. Its cross section is presented in Fig. 2.5. An n^+ buffer layer is incorporated between the n^- and the p^+ layer. The addition of an n^+ buffer causes an electric field with a trapezoidal shape; therefore, for a given blocking voltage, the PT-IGBT base width w_B is thinner than the base width of an NPT-IGBT structure. The n^+ buffer improves the turn-off speed by reducing the minority carrier injection. Besides, the latch-up characteristic is also improved by reducing the parasitic npn-transistor gain.

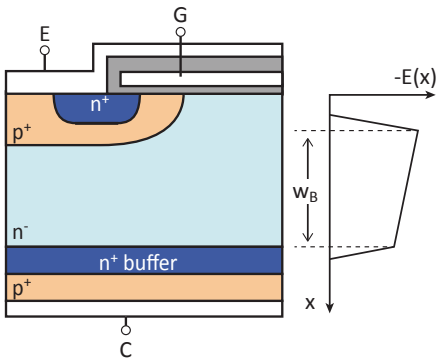


Figure 2.5: Representation of a PT-IGBT chip structure [6, 15].

PT-IGBTs are produced with an epitaxy process [6], where the n^+ buffer and the n^- layer are grown on a p^+ substrate.

Recently, new chip structures have been developed, such as Soft Punch Through (SPT-IGBT) and Trench-IGBT, in order to increase power density and ruggedness. These structures have been thoroughly described in the literature [6, 7, 10, 16, 17].

2.2 STATIC CURRENT-VOLTAGE CHARACTERISTIC

An IGBT output characteristic is presented in Fig. 2.6, where four different operation regions are identified (see e.g. [10]). Moreover, the figure shows the transfer characteristic $i_C = f(v_{GE})$ of the IGBT.

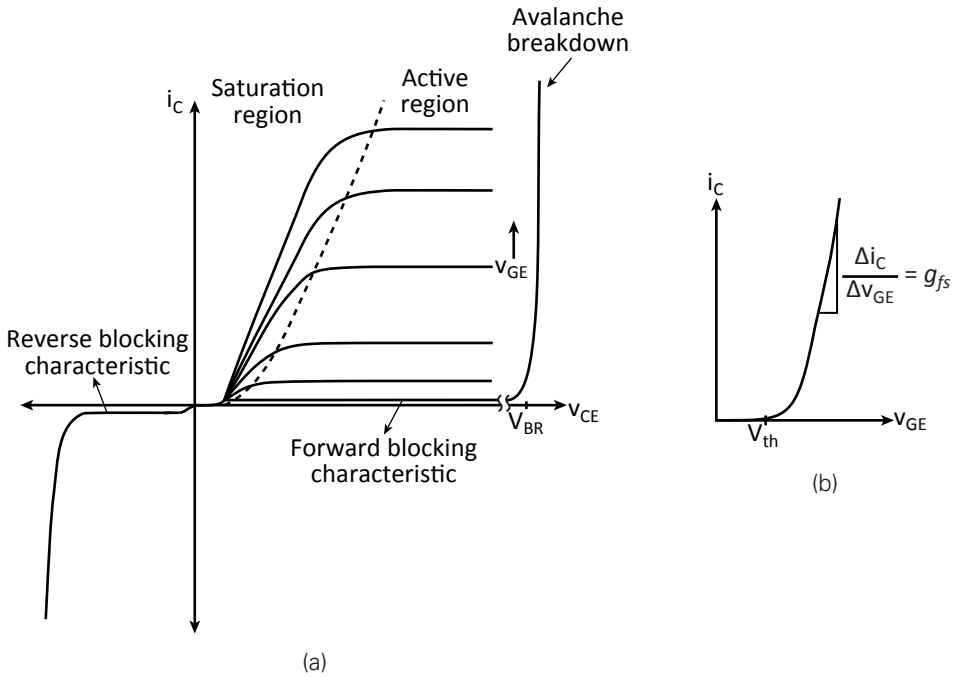


Figure 2.6: Representative curves of an IGBT [10]. (a) Output characteristics, and (b) transfer characteristic.

Reverse blocking characteristic: The reverse blocking characteristic of the IGBT is determined by the IGBT collector pn junction. The reverse current is close to zero, but increases rapidly when the collector-emitter voltage v_{CE} is close to the breakdown voltage of the collector pn junction.

In most applications the IGBT is connected with an anti-parallel diode, in order to allow current in the reverse direction. In these cases, the IGBT never blocks a large negative voltage. Therefore, a large reverse blocking capability is not needed [7]. However, for certain special applications reverse blocking IGBTs have been introduced on the market (e.g. [18–20]).

Saturation region: In this region, the IGBT is in the on-state, which is reached when the collector current is determined by the outer circuit. The MOS channel allows the injection of electrons into the n^- layer. The collector-emitter voltage is saturated ($v_{CE} \approx V_{CE,sat}$), since the n^- layer is flooded with bipolar charge carriers. In most modern IGBTs, the collector-emitter saturation voltage $V_{CE,sat}$ rises with the temperature, which is favourable for a parallel connection.

Active region: In this region, the collector current i_C is controlled by the gate-emitter voltage v_{GE} as:

$$I_{C,sat} = \frac{1}{1-\alpha_{pnp}} \cdot \frac{\kappa}{2}(v_{GE} - V_{GE,th})^2, \tag{2.1}$$

where $V_{GE,th}$ is the gate-emitter threshold voltage; κ is the channel conductivity and α_{pnp} is the pnp-transistor's current gain, which is generally less than 1 (0.2 to 0.3) [6].

The forward transconductance g_{fs} defined as:

$$g_{fs} = \frac{\Delta i_C}{\Delta v_{GE}}. \tag{2.2}$$

The forward transconductance increases in proportion to the collector current i_C and the collector-emitter voltage v_{CE}, and decreases as the IGBT temperature increases [10].

Forward blocking characteristic: In this region the gate-emitter voltage v_{GE} is lower than the threshold voltage $V_{GE,th}$. For a v_{CE} below the nominal voltage, the collector current is close to zero. When v_{CE} is close to the breakdown voltage the current increases rapidly with rising voltage. The leakage current is heavily dependent on the junction temperature T_j.

2.3 SWITCHING BEHAVIOUR

The switching behaviour of an IGBT is analysed using a buck converter as a test circuit, which is shown in Fig. 2.7. A detailed explanation of the switching process can be found in [6, 7, 9, 14, 21, 22].

2.3.1 Turn-on process

A typical turn-on transient is presented in Fig. 2.8, where the collector current, the collector-emitter voltage and the gate-emitter voltage are shown (e.g. [7]). Additionally, the figure shows an output characteristic, where the turn-on processes is depicted (dotted line). It is assumed as an initial condition that the load current i_L is circulating through the load L_L and the free-wheeling diode D ($i_D = i_L$). At t_0 the switch s_W changes from the position 1 to 2, initiating the turn-on process of the IGBT.

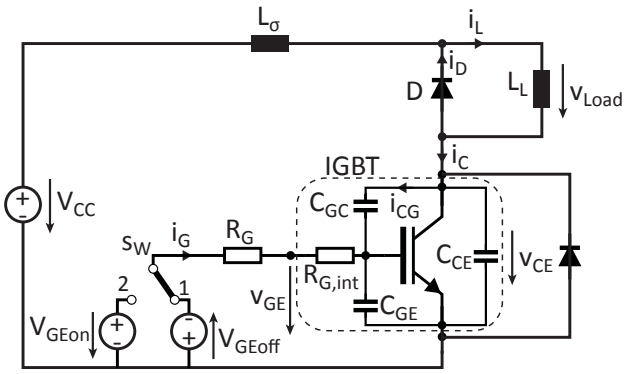


Figure 2.7: Test circuit to analyse the switching behaviour of the IGBT.

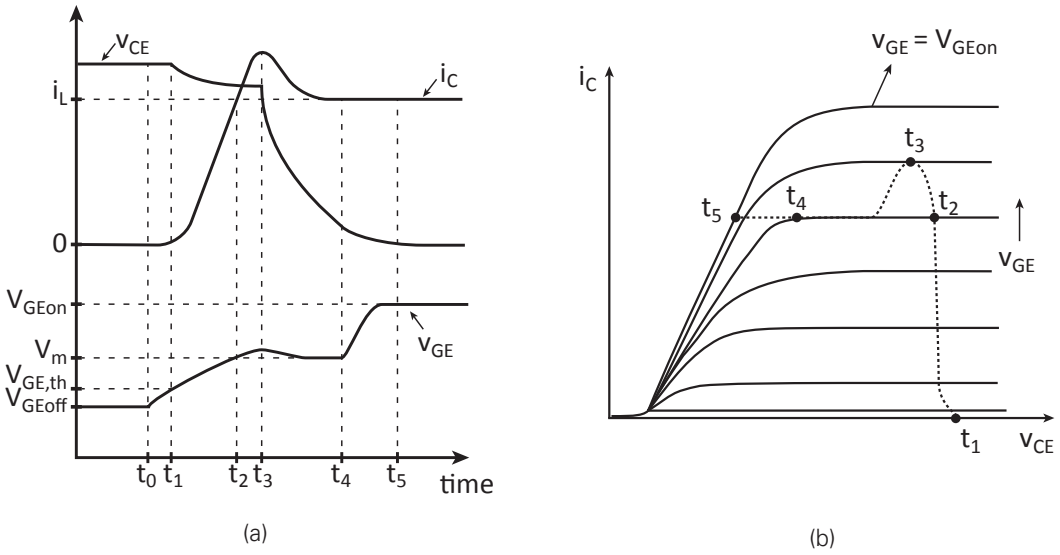


Figure 2.8: Turn-on transient process of an IGBT (e.g. [7]). (a) Collector current i_C, collector-emitter voltage v_{CE} and gate-emitter voltage v_{GE}, and (b) output characteristic.

Phase 1 ($t_0 - t_1$): The gate-emitter voltage v_{GE} increases from V_{GEoff} to the threshold voltage $V_{GE,th}$. The MOS channel has not been formed yet. Therefore, no electrons are injected into the n-region. The IGBT remains inactive. The gate-emitter voltage v_{GE} charges C_{GE} and C_{GC} through the total gate resistance $R_{G,tot} = R_G + R_{G,int}$. Thus, v_{GE} increases with a time constant defined by:

$$\tau_1 = R_{G,tot} \cdot (C_{GE} + C_{GC}(v_{CE})). \tag{2.3}$$

The IGBT's internal gate-collector capacitance (C_{GC}) value depends on the collector-emitter voltage v_{CE}. C_{GC} is reduced when v_{CE} increases and vice versa ($C_{GC} \sim 1/v_{CE}$).

Phase 2 ($t_1 - t_3$): The voltage v_{GE} has exceeded the threshold voltage $V_{GE,th}$. Therefore, the MOS channel is created and the collector current i_C starts to increase according to (2.2).

The collector voltage drops due to the induced voltage across the stray inductance L_σ:

$$v_{CE} = V_{CC} - L_\sigma \frac{di_C}{dt}. \tag{2.4}$$

After t_2, the load current i_L has been completely transferred from the free-wheeling diode D to the IGBT. Between t_2 and t_3 a reverse current flows through the diode.

Phase 3 ($t_3 - t_4$): The free-wheeling diode D is able to block voltage after t_3. Between t_3 and t_4 the gate-emitter voltage v_{GE} remains basically at a constant voltage V_m known as the Miller voltage. The entire gate current i_G discharges the IGBT's internal gate-collector capacitance C_{GC}. As a consequence, v_{CE} decreases and the value of C_{GC} increases simultaneously.

Phase 4 ($t_4 - t_5$): At t_4, v_{CE} has dropped to the level where the IGBT changes from the active to the saturation region. The voltage v_{GE} increases with a time constant given by (2.3). The turn-on transient is completed when v_{GE} reaches V_{GEon}.

2.3.2 Turn-off process

A typical turn-off transient is presented in Fig. 2.9, where the collector current, the collector-emitter voltage and the gate-emitter voltage are shown (e.g. [6, 7, 16]). At the beginning i_L flows through the load L_L and the IGBT ($i_C = i_L$). At t_0, the switch s_W changes from the position 2 to 1, initiating the turn-off process of the IGBT.

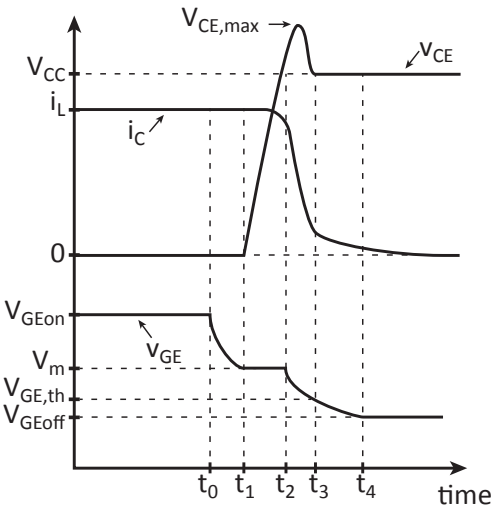


Figure 2.9: Turn-off transient of an IGBT (see e.g. [6, 7, 16]).

Phase 1 ($t_0 - t_1$): The gate-emitter voltage v_{GE} decreases from V_{GEon} to the Miller voltage V_m. The gate-emitter voltage v_{GE} is reduced with a time constant given by (2.3). During this phase there is basically no variation of v_{CE} and i_C.

Phase 2 ($t_1 - t_2$): v_{GE} reaches and remains at the constant voltage V_m. The collector-emitter voltage v_{CE} begins to increase. The value of C_{GC} decreases corresponding with the rise of v_{CE}. During this phase, the IGBT changes from the saturation to the active region. This phase is completed when v_{CE} reaches the DC-link voltage V_{CC}.

Phase 3 ($t_2 - t_3$): The collector current i_C decreases according to (2.2) and v_{GE} decreases with a time constant given by (2.3). A negative di_C/dt induces a negative voltage in the stray inductance L_σ. As a result a voltage overshoot occurs in the voltage v_{CE} according to (2.4). This phase is completed when voltage v_{GE} reaches the threshold voltage $V_{GE,th}$.

Phase 4 ($t_3 - t_4$): The IGBT's MOS channel is closed and the remaining holes in the n-region are removed by recombination. The tail current is a typical behaviour of a BJT and it has an important contribution to the turn-off losses.

2.4 SHORT CIRCUIT BEHAVIOUR

One of the main features of the IGBT is the capability to withstand a short circuit for a certain period of time. The basic short circuit behaviour of IGBTs is described in the literature e.g. [6, 7, 16, 22, 23]. During a short circuit, the rise of the collector current is limited by the gate-emitter voltage of an IGBT according to (2.1). Short circuits can be classified in two basic types:

- **Short circuit type I (SCI):** the IGBT is turned-on during an existing short circuit in the output circuit (e.g. load), and
- **Short circuit type II (SCII):** a short circuit occurs during the on-state of the IGBT [22].

An example of the SCI is shown in Fig. 2.10. At t_0, the IGBT is turned on and the collector current increases rapidly, which induces a voltage across the stray inductance L_σ, seen in the v_{CE} voltage drop between t_0 and t_1. At t_1, the collector current reaches its saturation value $I_{C,SCI}$ given by v_{GE} according to (2.1). The IGBT is operated in the active region with a high current, and therefore the IGBT heats up rapidly. The temperature negatively affects the channel mobility. Hence, the short circuit collector current decays slowly over the time. The GDU detects the short circuit condition and at instant t_2 the IGBT is turned off by reducing v_{GE} until $v_{GE} = V_{G,off}$. The high di_C/dt causes an over-voltage across v_{CE}. At t_3, the IGBT is turned off.

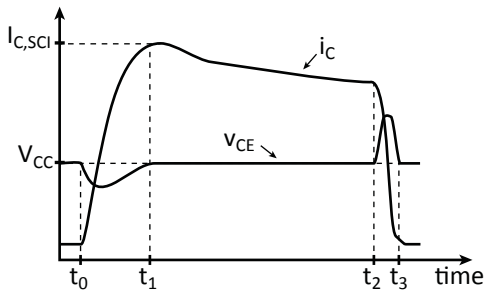


Figure 2.10: Example of a short circuit type I in an IGBT [7, 16, 22, 23].

If the IGBT is not turned off within the specified short circuit withstand time (usually 10 µs), the IGBT chip and/or the bond wires can melt due to the high power dissipation. In addition, the short circuit collector current can increase uncontrollably due to the latch-up of the parasitic thyristor which leads to the destruction of the semiconductor [7].

In case of SCII the IGBT carries the load current when the short circuit occurs. The collector current i_C increases rapidly with a $di_C/dt = V_{CC}/L_\sigma$. At a certain current level, the IGBT goes from the saturation to the active region. The voltage v_{CE} increases quickly and the dv_{CE}/dt influences the charge of C_{GC} with the current i_{CG} which will partly flow into the capacitance C_{GE}. The voltage v_{GE} increases, leading to a rise in i_C. The GDU should clamp the gate-emitter voltage, detect and turn off the short circuit current. A possible scheme of the short circuit detection and turn-off commands are discussed in Section 2.6.2.

2.5 PACKAGING OF HIGH-POWER IGBTS

The selection of the package type depends on the power range of the device. In the LV range, packages such as TO-series or SOT-series are generally used. In MV devices, press-pack (PP) and module housings are commonly applied.

2.5.1 Press-pack IGBTs

Fig. 2.11 shows a classic PP housing cross-section and a photo of a device. Traditionally, as for diodes and thyristors, the semiconductor wafer is mounted between two metal discs. The electrical and thermal contacts are established by applying pressure to the PP [24]. IGBT chips, on the other hand, are produced in small size ($< 300\,mm^2$), and therefore require several IGBT chips connected in parallel to achieve the desired current rating [6]. Ideally, all of the IGBT chips within the PP should be subjected to the same pressure in order to have an even current distribution through the whole device, which is a difficult task. One solution to this was proposed by IXYS UK Westcode, where each chip is mounted in a cell structure, as shown in Fig. 2.12 [25].

The PP IGBTs have advantages over module technology such as compact design, double-sided cooling and the lack of bond wires for the interconnection of the semiconductor dies. However, there is no separation between the current and heat flow paths. Besides, a high effort in the mounting assembly is needed, in order to keep a defined uni-axial mounting pressure.

Lately, the company ABB introduced the StakPak IGBT PP module [26] (see Fig. 2.13), where each chip is connected to the terminal by means of an individual spring, which allows to transfer the excess force to the housing wall.

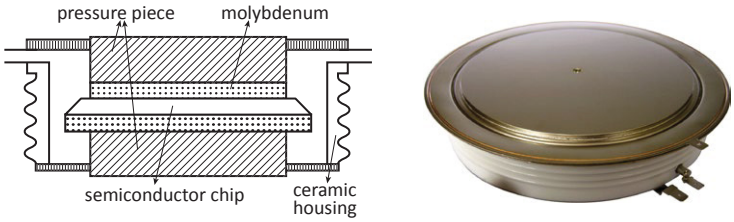


Figure 2.11: Press-pack housing cross-section (diodes, thyristors) and photograph [6].

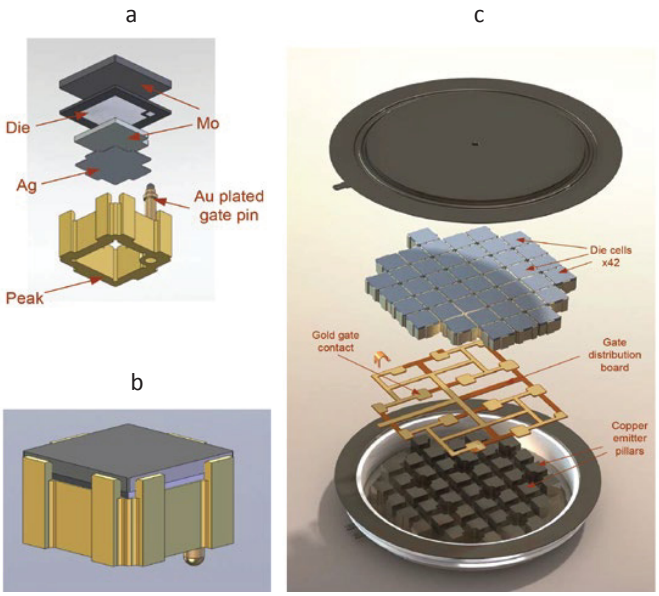


Figure 2.12: Internal construction of a PP IGBT [25].

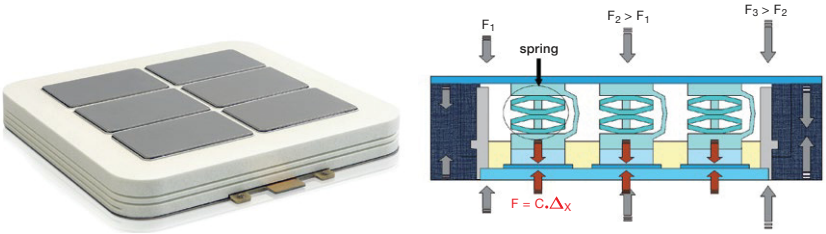


Figure 2.13: Internal structure and picture of a StakPak IGBT [26].

2.5.2 IGBT modules

Module housing was introduced by Semikron in 1975 [6]. It is characterized by separate current and heat flow paths. The internal insulation with good heat dissipation capability ensures an electrical isolation of the metal base plate from the power circuit. This isolation allows the connection of several IGBT modules working at different potentials to a common cooling plate [6, 10].

the cross-section of an IGBT module is presented in Fig. 2.14, where the top side of the IGBT chip is connected via aluminium bond wires to the copper surface. Robust load current terminals are soldered to the load current tracks of the ceramic substrate. Typical materials and thicknesses used in the construction of the IGBT modules are presented in Table 2.1.

Nowadays, a large variety of IGBT module housings can be found on the market. The type of module housing depends on the power of the device. Fig. 2.15 shows example of IGBT module housings from Infineon. A complete overview of the different modules can be found in [27].

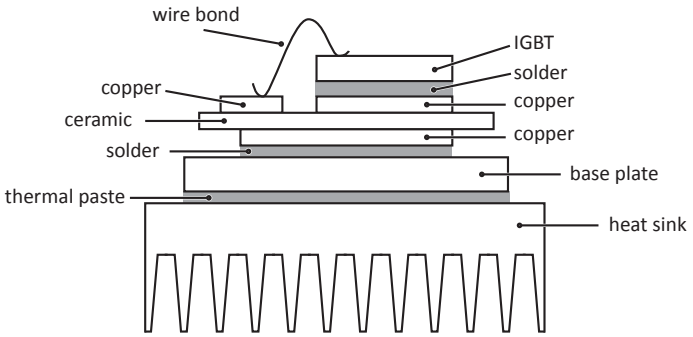


Figure 2.14: Cross-section of an IGBT module [6].

Table 2.1: Material and layer thickness of IGBT modules [6]

	Material, thicknesses (mm)	
Layer	Standard module	High-power module
Solder	0.05	0.05
Copper	0.3	0.3
Ceramic	[Al_2O_3] 0.381 - 0.635	[AlN] 0.635 - 1
Copper	0.3	0.3
Solder	0.1	0.1
Base plate	[Cu] 3	[Cu], [AlSiC] 5
Thermal paste	0.05	0.04

(a) (b) (c) (d)

Figure 2.15: Different types of IGBT modules of Infineon [27]. (a) EconoDUAL 3, (b) EconoPACK 4, (c) PrimePACK, and (d) IHV .

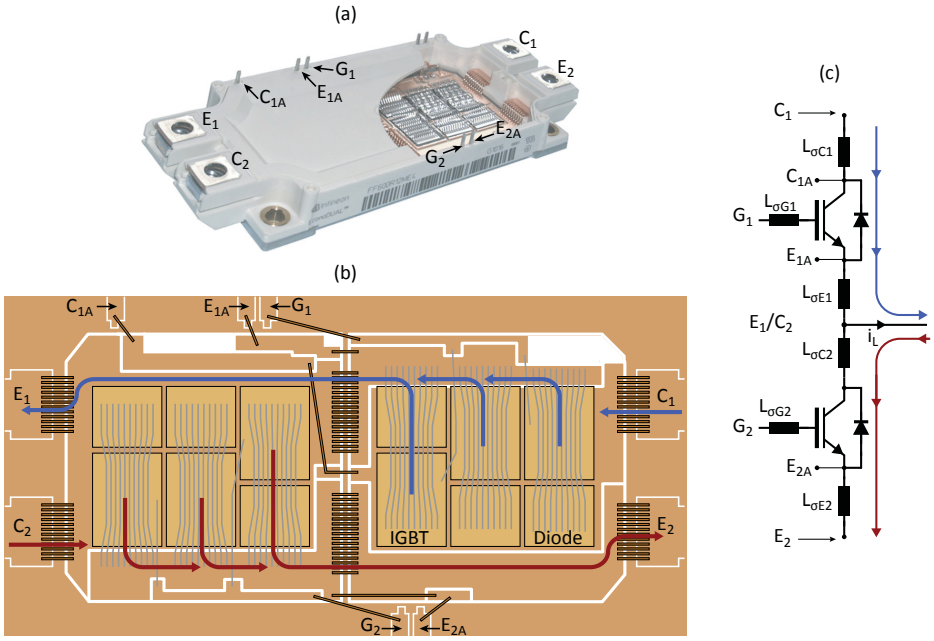


Figure 2.16: Dual IGBT EconoPACK layout. (a) IGBT module, (b) layout of the IGBT module, and (c) circuit diagram of the IGBT module.

The internal structure of a dual IGBT EconoPACK module is presented in Fig. 2.16. The internal parasitic inductances (stray inductances L_σ) in a module are the result of interconnections between the chips and the module terminals, where:

- $L_{\sigma G1}$ and $L_{\sigma G2}$ are stray inductances of the gate-emitter loop,
- $L_{\sigma C1}$ and $L_{\sigma C2}$ are stray inductances between the dies' collector terminal and the corresponding module's terminals, and
- $L_{\sigma E1}$ and $L_{\sigma E2}$ are stray inductances between the dies' emitter terminal and the corresponding module's terminals.

2.6 GATE DRIVE UNITS FOR IGBTS

An IGBT gate drive unit (GDU) or gate unit is an interface between the converter control unit and the IGBT, as shown Fig. 2.17. The trigger signals from the converter control unit are amplified by

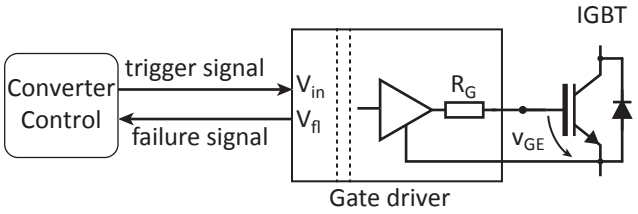


Figure 2.17: Scheme of the interaction of a GDU with the converter control and the IGBT.

increasing the voltage and current levels. In this manner, the input capacitances C_{GE} and C_{GC} are charged and discharged [16] in order to turn on and off the IGBT. Moreover, the GDU electrically isolates the converter control unit from the IGBT.

Nowadays, the GDU not only triggers the IGBT but also protects the device against short circuits and over-voltages. More advanced and complex GDUs allow the control of collector current *di/dt* and collector-emitter voltage *dv/dt* during the turn-on and turn-off transient. An overview thereof is presented in Section 5.3.

Typically, the GDUs output stages are based on a voltage source (VS). Hence, the power losses are dissipated in the gate resistances, in contrast with GDUs based on a current source (CS), where the losses are usually dissipated in the semiconductors of the driver stage.

2.6.1 Output stage circuit topologies

A GDU output stage with one power supply is studied in [28]. A summary of GDU circuits can be found in [16, 29–31]. The design and dimensioning of selected circuits is described e.g. in [32, 33]. In this section main GDU's output stage circuit topologies are presented.

2.6.1.1 Half-bridge with BJTs

The circuit topology is presented in Fig. 2.18. The v_{in} voltage switches between V_{GEon} and V_{GEoff}. The IGBT gate current i_G is limited by the gate resistances $R_{G,ON}$ and $R_{G,OFF}$. When v_{in} is equal to V_{GEon}, the BJT T_1 is turned on, and as a result the IGBT is turned on with a stationary voltage $v_{GE} \approx V_{GEon} - 0.7\,\text{V}$. When v_{in} is V_{GEoff}, the BJT T_2 is turned on and T_1 is turned off. Thus the IGBT is turned off with a stationary voltage $v_{GE} \approx -V_{GEoff} + 0.7$.

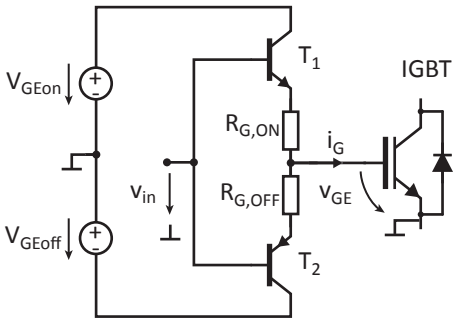


Figure 2.18: Half-bridge topology of a GDU output stage with BJT [16].

2.6.1.2 Half-bridge with MOSFETs

The circuit topology is shown in Fig. 2.19a. In this case, when v_{in} is positive (e.g. > 1 V), the MOSFET T_1 is turned on through the voltage level shifter Q_1 and the IGBT is also turned on through the gate resistance $R_{G,ON}$. When v_{in} is negative (e.g. < -1 V), the MOSFET T_2 is turned on through the voltage level shifter Q_2 and the IGBT is turned off through the gate resistance $R_{G,OFF}$. This configuration needs voltage level shifters Q_1 and Q_2, as the MOSFET gate-source voltage must be approximately 10 V, depending on the type of MOSFET) [16].

To avoid the voltage level shifters, a MOSFET push-pull configuration can be used, as presented in Fig. 2.19b. As an alternative, a bootstrap configuration can be used, as presented in [16, 34] and Section 5.4.1.

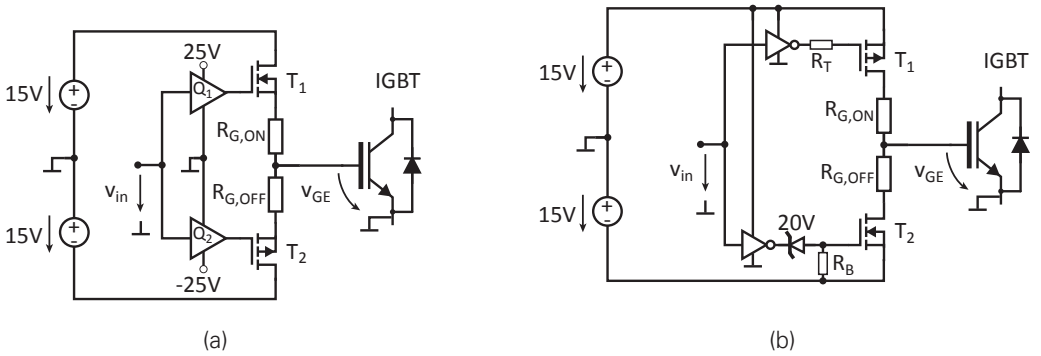


Figure 2.19: Half-bridge topology of a GDU with MOSFET [16]. (a) with, and (b) without voltage level shifters.

2.6.2 Protection circuits for IGBTs

An important task of GDUs is to protect the semiconductors against short circuits and collector-emitter v_{CE} over-voltages.

2.6.2.1 Short circuit protection

A protection scheme must be able to keep the IGBT safe during a short circuit e.g. of type I (SCI) and II (SCII), as defined in Sec. 2.4. A short circuit scheme can be based on the measurement of the collector current or the collector-emitter voltage v_{CE}. The collector current can be sensed by adding a shunt resistor in the current path [23, 35]. The voltage across this resistance provides a precise measurement of the current. However, the shunt resistor also generates losses, adds parasitic inductance which deteriorates the system performance and the response characteristic, which makes this an infeasible solution for high current.

The collector current can also be sensed with a current transformer, such as a Rogowski coil [36] or a Hall-effect sensors [23, 35]. These methods provide isolation between the power circuit and the protection circuit. However, these sensors are expensive, which makes an industrial implementation difficult.

As an alternative, the short circuit can be detected by sensing the collector-emitter voltage v_{CE} [16, 23, 37, 38]. A possible implementation of this solution is shown in Fig. 2.20. The v_{CE} voltage is sensed through the diode D_1 and the capacitor C_S, where the voltage across it ($v_S = v_{CE} + v_{D1}$) is acquired by the GDU.

When the IGBT is in on-state, it is saturated and the v_{CE} voltage is low and equal to $V_{CE,sat}$ (e.g. $\approx$3 V). This voltage increases in case of a short circuit, due to the desaturation of the IGBT. In this manner, the short circuit can be detected and the GDU turns off the IGBT. This method is effective and inexpensive.

In order to avoid an undesired increase of the gate-emitter voltage v_{GE} during a short circuit type II, a clamping circuit can be used. Zener diodes D_Z limit the gate-emitter voltage to a value lower than 20 V for example, and a Schottky diode D_C clamps v_{GE} to the power supply voltage, in this case 15 V.

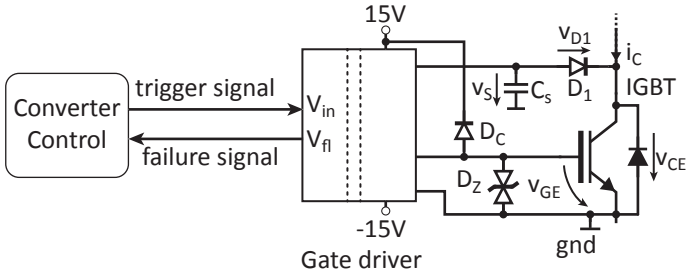


Figure 2.20: GDU short circuit protection scheme for IGBTs by sensing v_{CE} [16].

2.6.2.2 Collector-emitter over-voltage protection

During the turn-off transient, the high and negative di_C/dt induces a voltage across the stray inductances present in the commutation loop. The collector-emitter over-voltage, determined by (2.4), could exceed the breakdown voltage and destroy the IGBT. To mitigate the over-voltage, a snubber circuit can be used, but this adds volume and weight to the converter. Besides, the di_C/dt can be reduced by increasing the gate turn-off resistance in the GDU, at the cost of increasing the turn-off losses [23].

To overcome these problems, a GDU with an active clamping circuit can be used [16, 23, 37, 39]. One possible circuit is shown in Fig. 2.21.

While the IGBT is being turned off and as soon as the TVS diode D_{TVS} voltage is exceeded by v_{CE}, a current i_{TVS} flows through the diode D_{TVS}, which goes through the diode D_1 as i_{D1} and D_2 as i_{D2}. Part of the current i_{D1} goes through $R_{G,OFF}$ resistance. The current i_{D2} goes through the base of T_1 and through the base resistor R_B. As a consequence, the voltage v_{in} increases and becomes positive so that the transistor T_1 is turned on and T_2 is turned off. In this manner, the turn-off process is interrupted and v_{GE} is slightly increased, thus the di_C/dt as well as v_{CE} over-voltage are decreased during the turn-off transient of the IGBT.

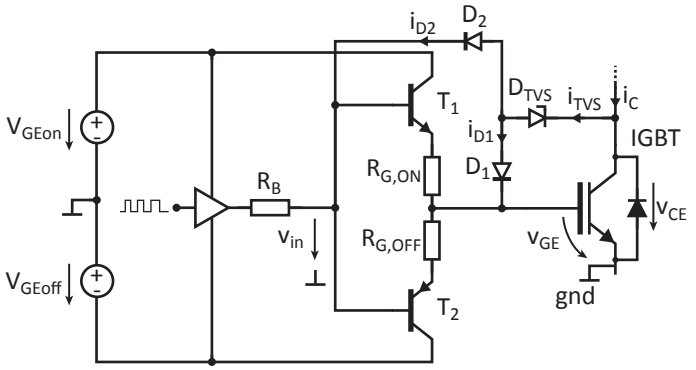


Figure 2.21: Example circuit for GDU over-voltage protection scheme for IGBTs using active clamping [16].

2.7 SUMMARY

This chapter presented an overview of IGBTs. The basic structure, function, and characteristics of common IGBTs were outlined. The on-state of the IGBTs and the switching transient phases were explained.

In addition, the fundamental IGBT behaviour under short circuit conditions was discussed. The different IGBT housings for high-power devices were presented and described. Furthermore, examples for the most used GDU topologies for the output stage, short circuit and over-voltage protection were described [16].

3 CURRENT ESTIMATION BY THE LEAKAGE EMITTER INDUCTANCE OF AN IGBT MODULE

This chapter presents novel schemes to estimate the collector current of IGBT modules based on the measurement of the voltage across its internal stray emitter inductance.

3.1 ESTIMATION OF THE COLLECTOR CURRENT

Figure 2.16 shows an equivalent circuit of a half bridge IGBT module. This section presents two new methods to estimate the collector current. Both methods are based on the measurement of the voltage across the parasitic leakage emitter inductance of an IGBT module. Compared to the leakage collector inductance, that of the emitter has the advantage that it is available for voltage measurements between the module terminals auxiliary emitter and power emitter and that the required electronic circuits can use the power supply of the corresponding IGBT GDU.

Both current estimation methods overcome the problems of the current measurement methods described in Section 2.6.2.1 with a simple scheme implemented in the GDU. The methods are called *current estimation by integration* (CEI) and *current estimation by comparison* (CEC), where the collector current is estimated by means of the sensed voltage v_{bond} across the stray emitter inductance L_{bond}, which is located between the auxiliary emitter and the power emitter as shown in Fig. 3.1.

These current estimation methods are frequently used throughout this thesis. They are used to determine the optimal parameters of RC-IGBTs (Section 4), to balance the collector current of parallel connected IGBTs, to detect short circuits and to improve the switching transients of IGBTs (chapter 5).

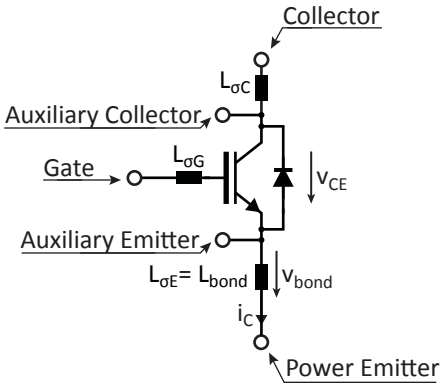


Figure 3.1: Equivalent circuit of an IGBT module and the internal stray inductances, $L_{\sigma C}$, $L_{\sigma G}$ and $L_{\sigma E} = L_{\text{bond}}$.

3.1.1 Current estimation by integration

The voltage v_{bond} across the stray inductance L_{bond} is proportional to the slope of the collector current i_C. Thus, the collector current i_C can be calculated as the integral of v_{bond} over a period of time as:

$$v_{\text{bond}} = L_{\text{bond}} \frac{di_C}{dt} \tag{3.1}$$

$$\triangle i_C = i_C(t_2) - i_C(t_1) = \frac{1}{L_{\text{bond}}} \int_{t_1}^{t_2} v_{\text{bond}}\, dt \tag{3.2}$$

An example of current estimation by using the integration of the voltage across the stray inductance v_{bond} is shown in Fig. 3.2. The collector-emitter voltage v_{CE} and a collector current i_C of the IGBT are shown in the top part of the figure. The collector current i_C induces a voltage v_{bond} across the stray inductance L_{bond}. With (3.2) the collector current i_C can be estimated, which is shown in the bottom part of Fig. 3.2 as $i_{C,\text{approx}}$. The integration limits t_1 and t_2 are obtained as the voltage v_{bond} falls below a low reference voltage $V_{\text{ref-off}}$. The estimated collector current $i_{C,\text{approx}}$ accurately follows an i_C waveform measured with a Rogowski coil. In this case, the value of the stray inductance L_{bond} is around 12 nH.

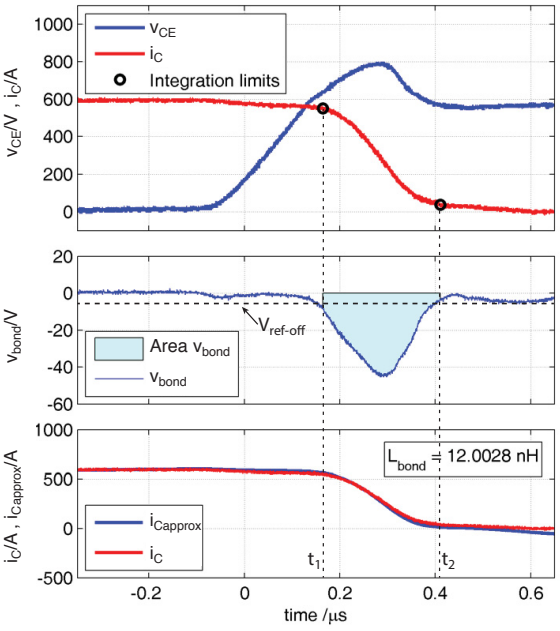


Figure 3.2: Example of the current estimation by integration using the voltage across the module's emitter stray inductance (V_{CC} = 600 V, I_C = 600 A, T_j = 25°C).

An implementation of the method is shown in Fig. 3.3. The voltage across the stray inductance v_{bond} is measured during the turn-off transient of the IGBT in order to avoid the reverse recovery effect. The sensed voltage $v_{\text{bond,i}}$ is integrated by an analog integrator with reset. After the integration period, the integrated voltage i_{int} is sampled with a 12-bit analog-to-digital converter (ADC) and transmitted to a field-programmable gate array (FPGA) via a capacitive isolator as the signal $i_{\text{int,i}}$.

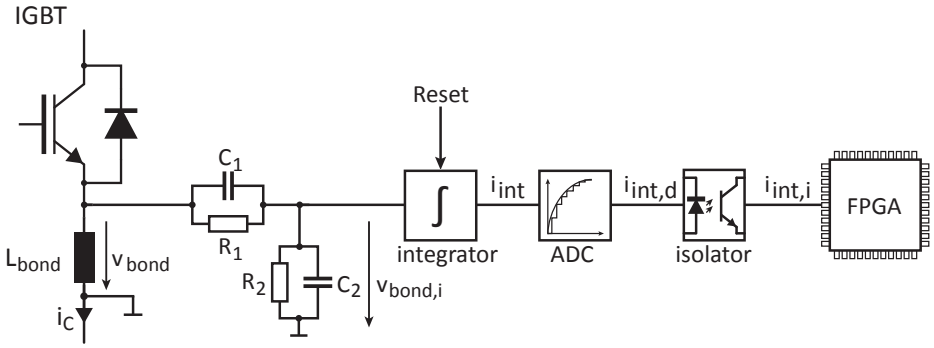


Figure 3.3: Schematic of the proposed current estimation by integration method.

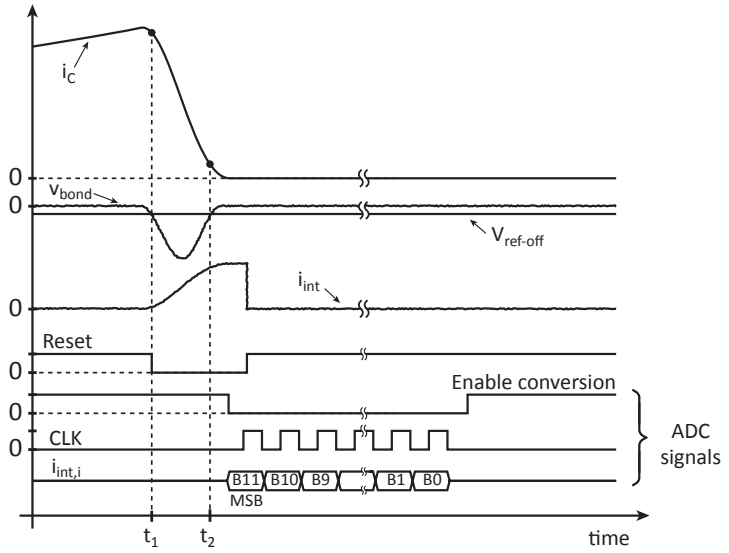


Figure 3.4: Ideal waveforms of the process of the current estimation by integration method, including ADC signals.

The integration process is presented in Fig. 3.4. The reset signal is controlled by the FPGA, and as long as the signal is on (logic value as 1), the integration will not take place. During the turn-off transient the reset signal is set to zero for a time window $\Delta t = t_2 - t_1$. This window is obtained by comparing v_{bond} with a low reference voltage ($V_{\text{ref-off}}$). After the integration time t_2, the FPGA enables the conversion into a digital signal with a 12-bit ADC which sends the digital value to the FPGA as $i_{\text{int,i}}$. An algorithm uses this information to estimate the collector current.

3.1.2 Current estimation by comparison

The collector current can also be estimated by comparing v_{bond} with a threshold value during the turn-on transient (*ON comparison method*) and during the turn-off transient (*OFF comparison method*). The voltage across the stray inductance v_{bond} is proportional to the slope of the collector current, as shown in (3.1). By applying the sign function to (3.1), it is possible to obtain information about whether the collector current is increasing (turn-on transient) or decreasing (turn-off transient) [40].

$$\text{sgn}\left(\frac{v_{\text{bond}}}{L_{\text{bond}}}\right) = \text{sgn}\left(\frac{di_{\text{C}}}{dt}\right) \tag{3.3}$$

The principle of the collector current estimation by comparison is shown in Fig. 3.5. The voltage across the stray inductance v_{bond} is sensed and compared with low threshold values, $V_{\text{ref-on}}$ and

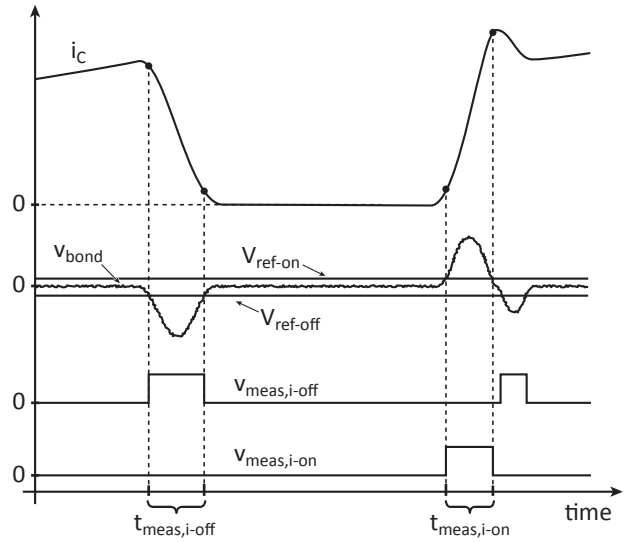


Figure 3.5: Ideal waveforms of the operation of the current estimation by comparison.

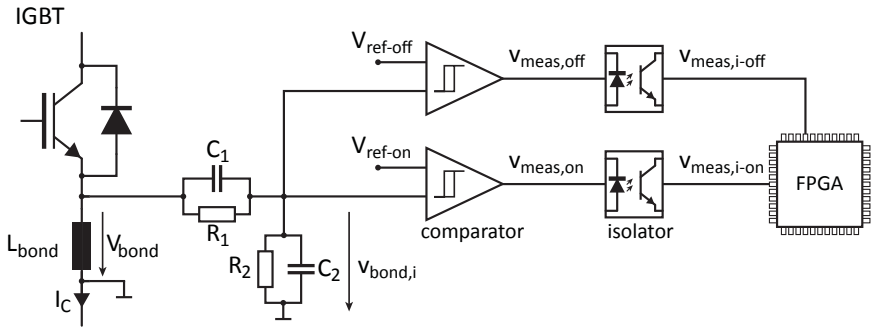


Figure 3.6: Possible implementation of the proposed current estimation by comparison.

$V_{\text{ref-off}}$, in order to approximate the sign function during the turn-on and turn-off transient respectively. Two binary signals are generated, $v_{\text{meas,i-on}}$ and $v_{\text{meas,i-off}}$ (during the turn-on transient is $v_{\text{meas,i-on}} = 1$ and during the turn-off transient is $v_{\text{meas,i-off}} = 1$). The pulse length represents the period in which the threshold voltages have been exceeded (positive *di/dt*) or fallen bellow (negative *di/dt*), which are defined as $t_{\text{meas,i-on}}$ for the ON comparison method and $t_{\text{meas,i-off}}$ for the OFF comparison method. Estimation of the collector currents based on measurements of these pulse length is discussed further in Section 3.2. In case of the ON comparison method the reverse recovery current is included in the estimation ($i_C + i_{\text{RRM}}$).

Figure 3.6 shows a block diagram of one feasible implementation of this current estimation method, where v_{bond} is measured by a compensated voltage divider and compared with two small reference values, $V_{\text{ref-on}}$ and $V_{\text{ref-off}}$ [40]. The output signals of the comparators are galvanically isolated and sent to the control stage (e.g. FPGA) as $v_{\text{meas,i-on}}$ for the turn-on transient and $v_{\text{meas,i-off}}$ for the turn-off transient. An algorithm extracts their time information, $t_{\text{meas,i-on}}$ and $t_{\text{meas,i-off}}$, and estimates the collector current.

3.2 CURRENT ESTIMATION ALGORITHM

A block diagram of the current estimation algorithm is shown in Fig. 3.7, which is divided into three stages:

- **Extraction of the time information:** The algorithm extracts the time information, $t_{meas,i\text{-}on}$ and $t_{meas,i\text{-}off}$, for the current estimation method by comparison. With this information the current can be estimated.
- **Calibration algorithm:** With this stage the current estimation methods are calibrated. Thus, the values of L_{bond} and di_C/dt do not need to be known for the algorithm to work.
- **Estimation of the current:** The collector current i_C is estimated by linear interpolation.

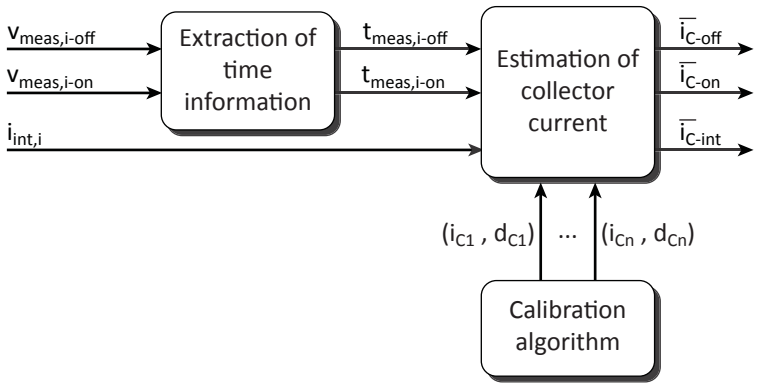


Figure 3.7: Block diagram of the current estimation algorithm.

3.2.1 Extraction of time information

A block diagram of the algorithm is presented in Fig. 3.8. This block is implemented only for the current estimation method by comparison. An increasing counter runs as long as the binary signals $v_{meas,i\text{-}on}$ and/or $v_{meas,i\text{-}off}$ are high. When $v_{meas,i\text{-}on}$ and/or $v_{meas,i\text{-}off}$ have a high to low transition, the count of the counter is assigned to $t_{meas,i\text{-}on}$ for the turn-on transient and/or $t_{meas,i\text{-}off}$ for the turn-off transient. The resolution of this method depends on the speed of the counters, which depends on the clock frequency of the FPGA. A faster FPGA will provide better resolution.

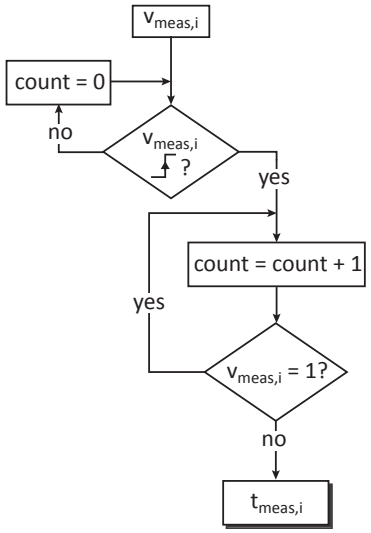


Figure 3.8: Block diagram of the extraction of the time information.

3.2.2 Calibration algorithm

The methods CEI and CEC are calibrated in order to be independent of the values of the stray inductance L_{bond}, di_C/dt, gate-resistances, the gate-emitter threshold voltage of the IGBT and the tolerance of the electronic circuitry components. In the calibration process, the signals $i_{int,i}$, $v_{meas,i\text{-}on}$ and $v_{meas,i\text{-}off}$ are acquired at different current levels, which are generated with a double pulse test defined as follows.

Double pulse test definition: The test circuit is a buck converter, as Fig. 3.9a shows. The IGBT is operated in the so-called double pulse mode by the signal s_1. Initially the collector current i_C increases linearly through the IGBT, allowing the characterization of the switching behaviour of the IGBT and the diode at different operating currents. The junction temperature T_j of the DUT can be controlled externally to perform the test at different values. Fig. 3.9b shows example waveforms of a double pulse test. The collector current amplitude is controlled by adjusting the turn-on time $\Delta t = t_1 - t_0$. After this period of time the IGBT is turned off and the measurement of the collector current and the collector-emitter voltage allow the IGBT turn-off transient characterization. During the period of time between t_1 and t_2 the diode is in conduction state. At t_2 the IGBT is turned on and the turn-on behaviour of the IGBT and the turn-off behaviour of the diode are characterized.

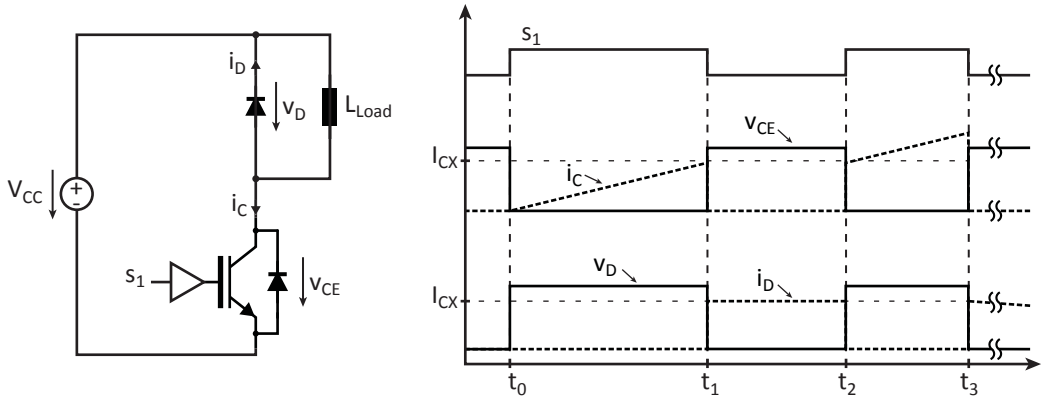


Figure 3.9: Double pulse test definition. (a) circuit test, and (b) waveforms.

The calibration algorithm block diagram is shown in Fig. 3.10. Different current levels are generated by modifying the first pulse of the double pulse test according to:

$$\Delta t \;=\; t_1 - t_0 \;=\; \frac{L_{Load}}{V_{CC}} \cdot I_{Cx}, \tag{3.4}$$

where I_{Cx} (with x= 1...n) is the desired collector current for a given V_{CC} and L_{Load}. After every double pulse test the signals of each estimation method $i_{int,ix}$, $v_{meas,i\text{-}onx}$ and $v_{meas,i\text{-}offx}$ are acquired. The algorithm extracts the value of $i_{int,ix}$ and the corresponding time information $t_{meas,i\text{-}onx}$ and $t_{meas,i\text{-}offx}$. These values are assigned to $d_{Cx\text{-}i}$, $d_{Cx\text{-}on}$ and $d_{Cx\text{-}off}$ respectively. The algorithm maps values of $d_{Cx\text{-}i}$, $d_{Cx\text{-}on}$ and $d_{Cx\text{-}off}$ to the corresponding current amplitude (I_{Cx}), creating three look-up tables, one for each acquired signal. This algorithm is added in a start-up routine. Fig. 3.11 shows an example of one of the three look-up tables with eight calibration points.

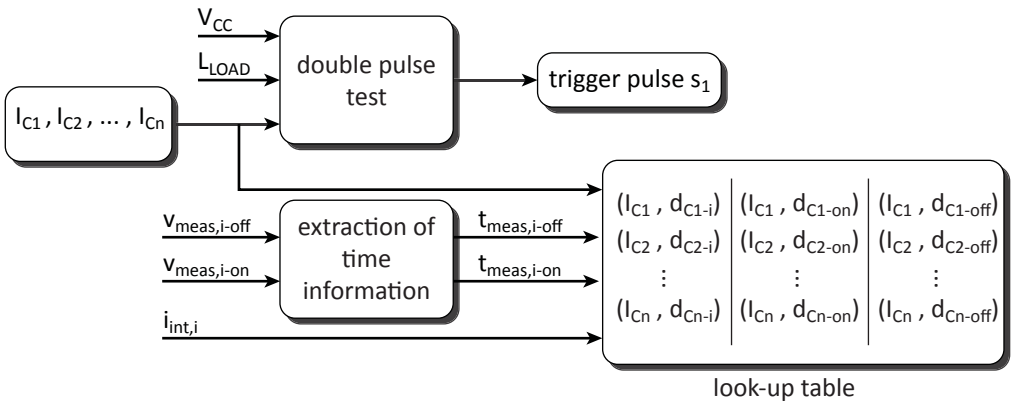


Figure 3.10: Block diagram of the algorithm to calibrate the current estimation methods.

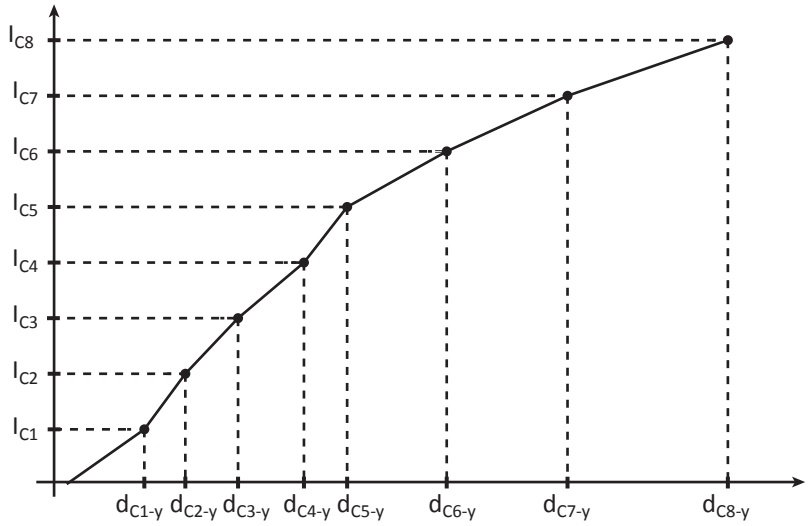


Figure 3.11: Example of the virtual graph created after the calibration of the current estimation method. I_{CX}: collector current generated with the double pulse test, x = 1...8. $d_{CX\text{-}y}$: collector current value of the estimation methods (y = i, on and off).

3.2.3 Estimation of the current

During the operation of the IGBT, the collector current is estimated with a linear interpolation using the two closest points from the calibration process as described in (3.5), where $\overline{i_{Cm}}$ is the estimated current; $\overline{d_{Cm}}$ is the acquired value from the current estimation methods ($i_{int,i}$, $t_{meas,i\text{-}on}$ or $t_{meas,i\text{-}off}$); $(d_{C(m+1)}, I_{C(m+1)})$ and $(d_{C(m-1)}, I_{C(m-1)})$ are the closest points given by the calibration process, as shown in Fig. 3.12.

$$\overline{i_{Cm}} = \begin{cases} \dfrac{I_{C1}}{d_{C1}} \cdot \overline{d_{Cm}} & , \overline{d_{Cm}} < d_{C1} \\ \dfrac{I_{C(m+1)} - I_{C(m-1)}}{d_{C(m+1)} - d_{C(m-1)}} \cdot \overline{d_{Cm}} + I_{C(m-1)} & , d_{C1} \leq \overline{d_{Cm}} \leq d_{Cn} \end{cases} \tag{3.5}$$

If $d_{Cm} > d_{Cn}$ the system must be re-calibrated with a wider range of collector currents values. The maximal collector current during the calibration process ($\widehat{I_{C,cal}}$) should be twice the IGBT nominal current ($\widehat{I_{C,cal}} = 2 \cdot I_{CN}$).

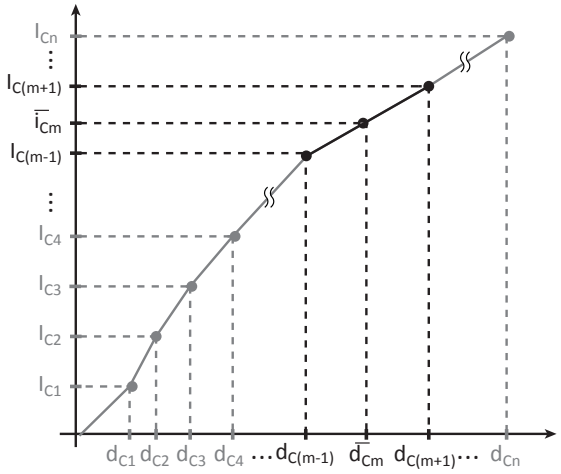


Figure 3.12: Example of the estimation of the current by using the virtual graph.

3.3 EXPERIMENTAL VERIFICATION

The collector current estimation methods have been implemented in a GDU as shown in Fig. 3.13 and were experimentally verified using a buck converter. The GDU was designed for a half-bridge IGBT module. A block diagram of the GDU is presented in Fig. 3.14, where the interconnections between FPGA and the GDU are shown. The main requirement to the GDU was the verification of the basic operation principle and the estimation of the accuracy of the principle. The block diagram can be divided in 5 stages:

- **Communication Stage:** It connects the gate unit with the FPGA through cat 5e cables and high speed differential drivers.
- **Isolation Stage:** It isolates the control signal to the GDU signals. The isolators feature 560 V isolation and support data transfer rates up to 150 Mbps.
- **Power Supply:** An adjustable DC-DC converter is implemented in order to regulate the output voltage.
- **Power Stage:** The IGBT is turned on and off using a push-pull amplifier.
- **Measurement Stage:** The current estimation methods are implemented. The FPGA counts the length of $V_{meas,i\text{-}on}$ and $V_{meas,i\text{-}off}$ at 200 Mhz.

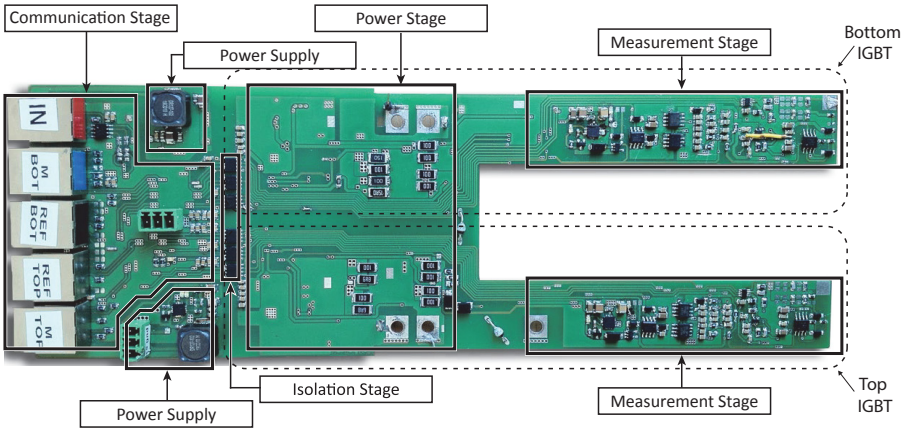


Figure 3.13: Gate unit PCB prototype for the verification of the current estimation methods.

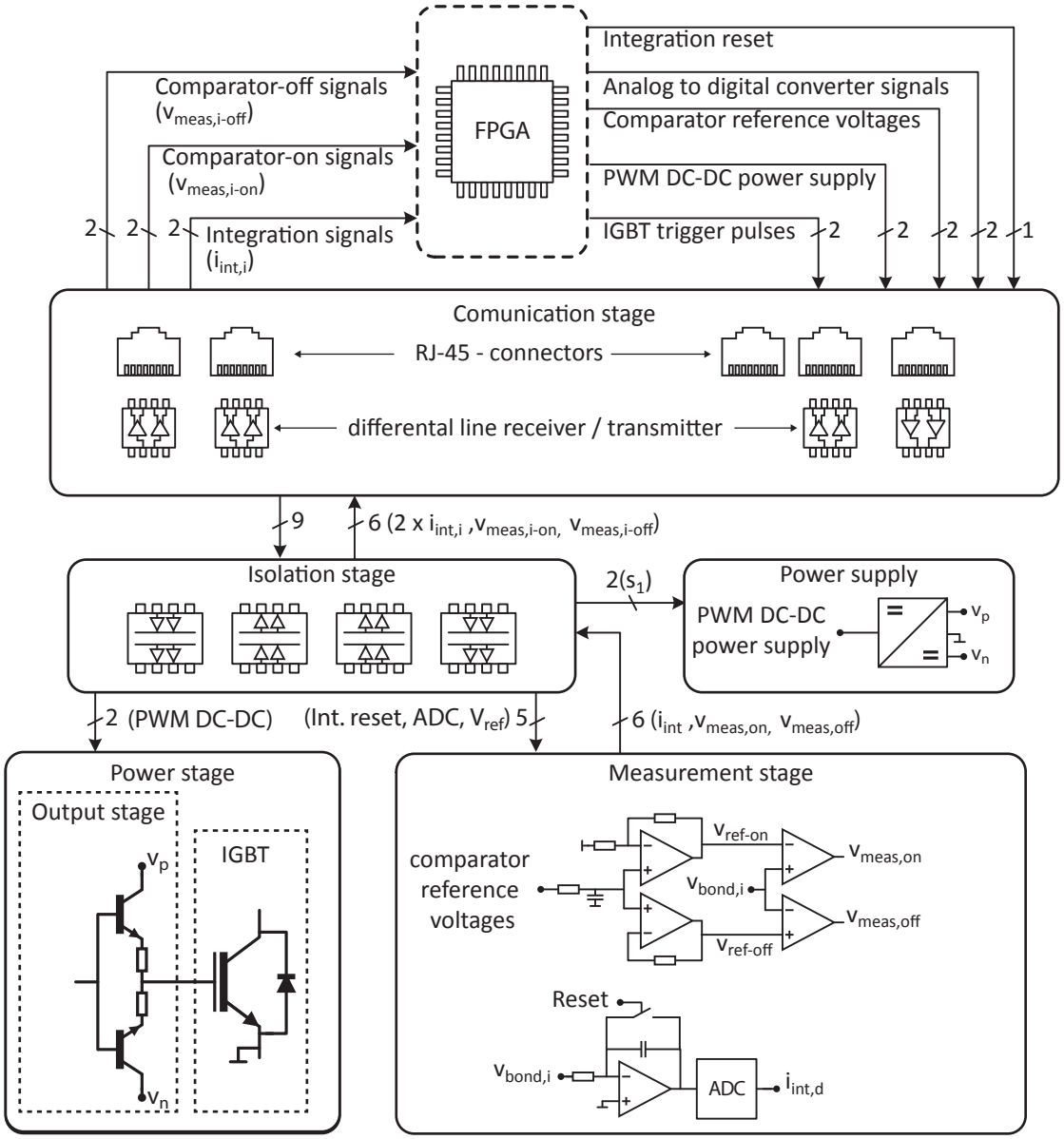


Figure 3.14: Block diagram of the GDU for verifying the current estimation methods.

3.3.1 Test description

The current estimation methods are tested in a buck converter, as shown in Fig. 3.15. The experimental conditions are listed in Table 3.1.

3.3.2 Experimental results

The results of the calibration process of the current estimation methods are shown in Fig. 3.16, Fig. 3.17 and Fig. 3.18. The virtual graphs are created with eight calibration points, where the collector current is modified from 50 to 400 A in steps of 50 A. The ON comparison method (Fig. 3.16) and the integration method (Fig. 3.18) resulted in a linear relation of $t_{meas,i\text{-}on}$ and $i_{int,i}$ to the collector current. However, the OFF comparison method (Fig. 3.17) suffered from resolution

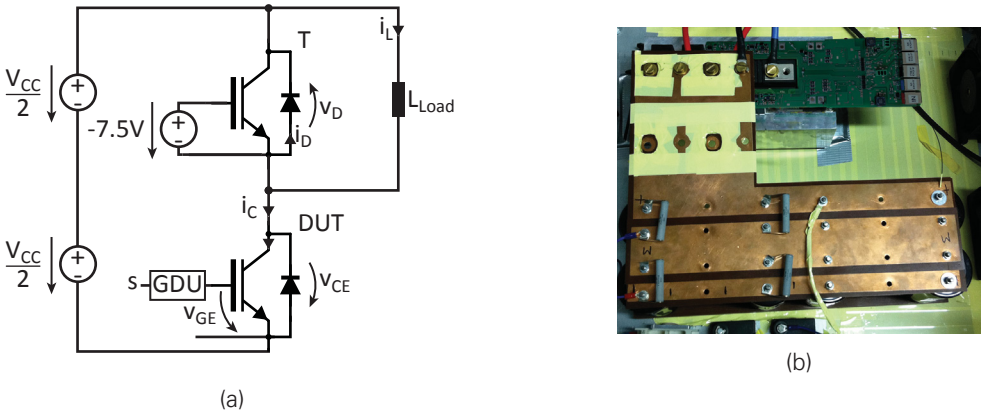


Figure 3.15: Setup used for the test of the current estimation methods. (a) Circuit topology, and (b) picture of the setup.

Table 3.1: Test conditions for the verification of the current estimation methods

Variable	Value
Mode of operation	Double pulse test
IGBT	FF650R17IE4 (650 A / 1700 V)
V_{CC}	100...300 V
i_C	50...400 A
T_j	25 °C

problems for current levels between 150 A and 250 A, where the FPGA count ($t_{meas,i\text{-}off}$) changes only from 28 to 31, which results in a large error during the estimation process.

The performance of the current estimation methods is tested by comparing the estimated collector current with the collector current measured with a Rogowski coil. The estimation error is defined as:

$$E_R = \left| \frac{I_C - \overline{i_{Cm}}}{I_C} \right|, \tag{3.6}$$

where $\overline{i_{Cm}}$ is the estimated collector current and I_C is the measured collector current. The results are shown in Fig. 3.19. The methods were tested at 200 V. The ON comparison and the integration methods demonstrated an error less than 8% for currents over 150 A. The OFF comparison method resulted in an error up to 75% between 150 and 300 A due to the low resolution during the calibration process.

The current estimation methods are distinctly less precise than the conventional current measurement sensors such as Shunt resistors, Hall-effect sensors or Rogowski coils (which have typical errors of <1%). Advantages of the proposed current estimation methods are their simplicity and cost, which make these solutions attractive for industrial applications. Potential first applications are discussed in the following chapters.

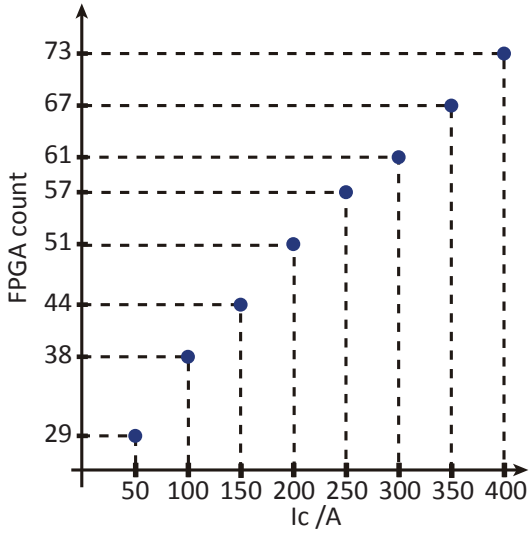


Figure 3.16: Calibration graph of the ON comparison method. Current estimation values obtained by the FPGA (FPGA count) at different collector current values (V_{CC} = 300 V, T_j = 25°C).

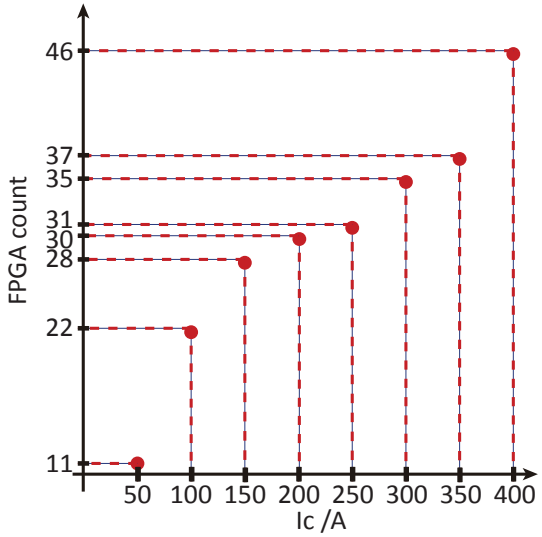


Figure 3.17: Calibration graph of the OFF comparison method. Current estimation values obtained by the FPGA (FPGA count) at different collector current values (V_{CC} = 300 V, T_j = 25°C).

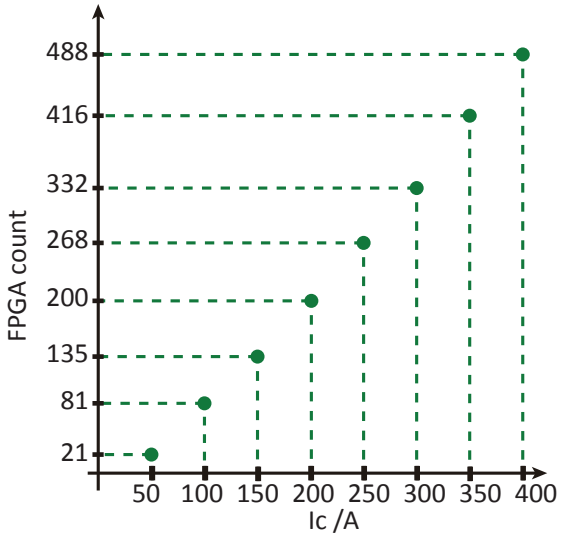


Figure 3.18: Calibration graph of the method current estimation by integration. Current estimation values obtained by the FPGA (FPGA count) at different collector current values (V_{CC} = 300 V, T_j = 25°C).

3.4 CURRENT ESTIMATION OF PARALLEL CONNECTED IGBTS

A current measurement or current estimation method is a basic requirement for active static current balancing of IGBTs connected in parallel, as discussed in Sec. 5.1. Therefore, the methods are tested in a buck converter with two IGBTs connected in parallel as shown in Fig. 3.20.

The current is estimated with the ON comparison method, due to its simplicity and performance ($E_R < 8\%$). The results of one experimental trial are shown in Fig. 3.21a as an example. The collector current had a double overshoot during the turn-on transient due to the reverse recovery current of the not ideally switching complementary diodes connected in parallel. This double peak is a problem for the ON comparison method during the calibration process, and, hence, for the

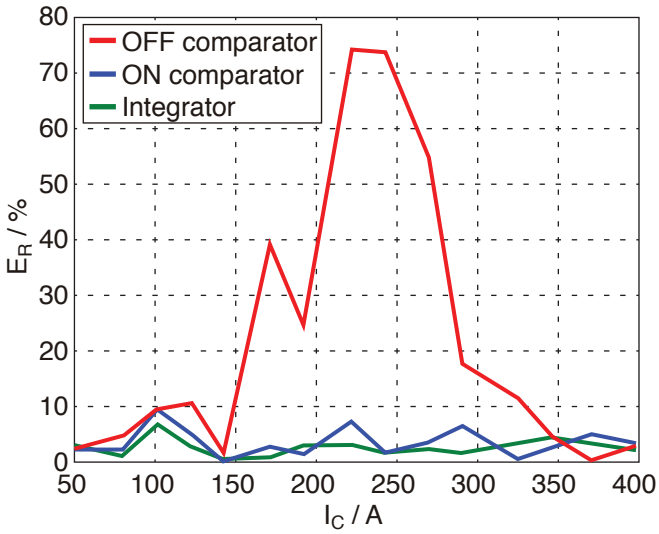


Figure 3.19: Error of the current estimation methods, obtained during experimental verification (V_{CC} = 200 V, T_j = 25°C).

estimation of the collector current. Therefore, the collector current should be estimated during the turn-off transient, which should be done with the integration method, since it has lower error. However, the integrator needs extra hardware compared to the ON comparison method. The OFF comparison method could be an alternative when a faster FPGA is used in order to avoid problems related to the low resolution.

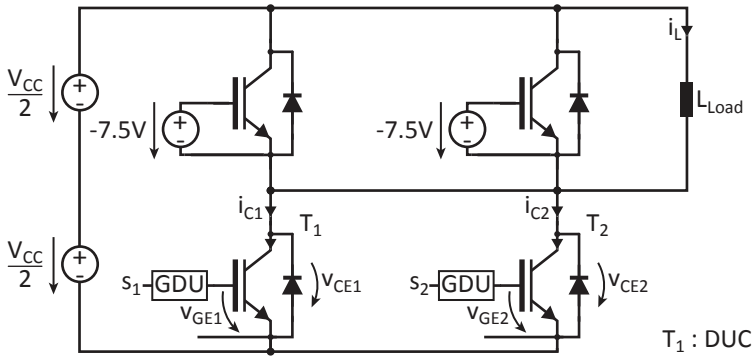


Figure 3.20: Buck converter used for the calibration of the current estimation methods for IGBTs connected in parallel. DUC: device under calibration.

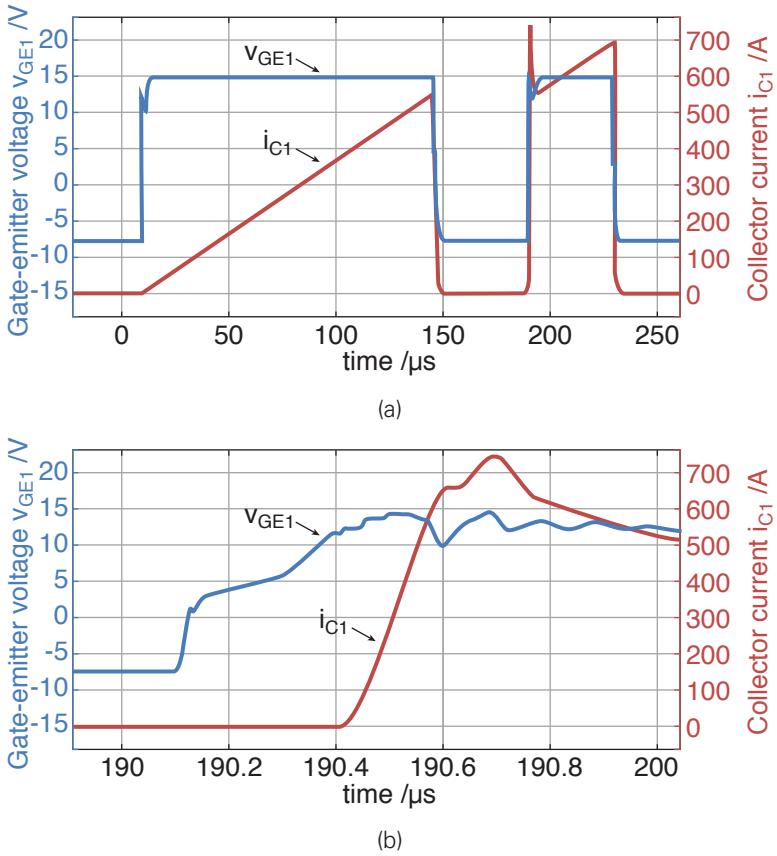


Figure 3.21: Turn-on transient during the calibration process of the current estimation methods for IGBTs connected in parallel (V_{CC} = 500 V, I_C = 550 A T_j = 25°C).

3.5 SUMMARY

This chapter presented two novel methods for estimating the collector current of IGBT modules, which are based on the measurement of the voltage v_{bond} across the stray inductances L_{bond} located between the auxiliary emitter and the power emitter. An implementation scheme of the methods is also included.

Both methods need calibration, which consists of a double pulse test at various currents. In an industrial converter this double pulse test could be realized within the first converter test at the manufacturer, e.g. within a start up routine for a converter. Once the methods have been calibrated, the collector current is estimated with a linear interpolation using the two closest points given by the calibration process.

Experimental results showed that the current estimation error with the integration and ON comparison method can be lower than 8%. The current estimation by the OFF comparison method had substantial measurement error (e.g. up to 75%), due to resolution problems during the calibration, although it has the same resolution as the ON comparison method. This result could be improved by the use of a faster FPGA. Finally, the calibration process of two parallel IGBT modules was shown, which is a more challenging case due to the double current peak during the turn-on transient.

4 REVERSE CONDUCTING IGBTS

4.1 STRUCTURE, FUNCTION AND CHARACTERISTICS

In voltage source converters, IGBTs are usually connected with an anti-parallel diode. This configuration enables a separate optimization of IGBT and diode. Reverse conducting IGBTs (RC-IGBTs) have been developed to increase the silicon utilization, to increase the over-current capability of the diode (e.g. I^2t-value) and to improve the power and thermal cycling capability of IGBT modules [41].

Reverse conducting IGBTs integrate an IGBT and an anti-parallel diode into the IGBT cell, as shown in Fig. 4.1. An RC-IGBTs can operate as an IGBT (e.g. in forward conduction mode) or as a diode (e.g. in reverse conduction mode).

Presently, several companies produce RC-IGBTs, but they are mainly low power semiconductors for applications such as inductive cooking stoves, microwaves, rice cookers, printers, refrigerators, etc. A market overview of RC-IGBTs is listed in Table 4.1.

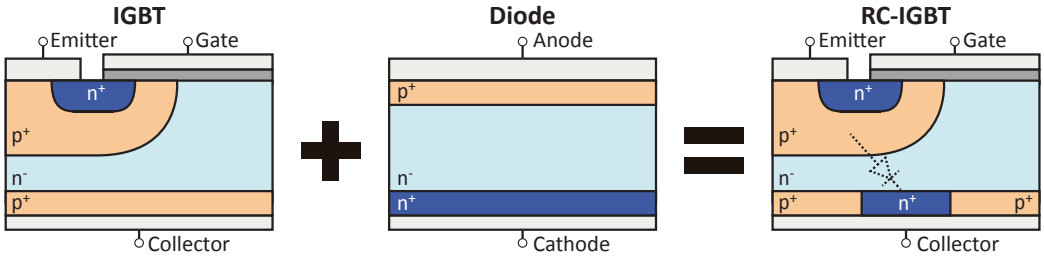


Figure 4.1: Chip structure of IGBT, diode and RC-IGBT.

Other companies, such as Fuji and ABB, have also been investigating the potential of RC-IGBTs. Fuji has produced a 100 A / 1200 V RC-IGBT prototype with a new compact package [42]. ABB has been investigating an advanced RC-IGBT concept, named bi-mode insulated-gate transistor (BIGT) [43]. The prototype is a module with 2000 A / 3300 V capability.

As the RC-IGBT can operate as an IGBT, standard modulation strategies such as PWM and space vector modulation can be applied. However, when the RC-IGBT is in the reverse conduction mode, the MOS-channel of the RC-IGBT should maintained in a non-conductive state ($v_{GE} \leq V_{GE,th}$) to decrease the on-state losses [11, 44, 45]. The direction of the current conduction, that

Table 4.1: Market overview of commercially available RC-IGBTs

Company	Ratings (V_{CE} / I_C)	Package
Infineon	600 V / 2.5 ... 40 A	TO-247, DPAK
	650 V / 20 ... 50 A	TO-247
	1100 V / 30 A	TO-247
	1200 V / 15 ... 40 A	TO-247
	1200 V / 15 ... 40 A	TO-247
	1350 V / 20 ... 40 A	TO-247
	1600 V / 30 A	TO-247
IXYS	1600 V / 5.7 ... 28 A	TO-220, TO-247, ISOPLUS i4-PAC
	1700 V / 10 ... 200 A	TO-268, TO-247AD, TO-264, SOT-227B
	2500 V / 5 ... 156 A	TO-268, TO-247, TO-264, ISOPLUS I5-PAK
	3000 V / 26 ... 130 A	TO-268, TO-247, TO-263, TO-264, ISOPLUS I4-PAK
	3600 V / 45 ... 125 A	TO-247HV, TO-268HV, ISOPLUS I5-PAK, ISOPLUS I5-PAK
Mitsubishi	600 V / 15 A	SLIMDIP-L

is, either forward or reverse, can be detected based on a measurement of the collector-emitter voltage [11, 45] or its variation (e.g. dv_{CE}/dt) attained by means of a measurement of the gate current [44].

The RC-IGBT, in reverse conduction mode, presents a high reverse recovery current peak compared to a standard diode. Different solutions have been proposed in the literature to overcome this problem either by modification of the semiconductor device itself [46] or of the gate driving scheme [12]. The reverse recovery peak can be reduced by device modification by the application of a charge-carrier lifetime control technique. Possibilities for charge carrier lifetime control are e.g. irradiation with particles such as electrons, protons or helium ions, or the diffusion of a heavy metal such as platinum. However, the exposure to particles also causes undesirable charges in the gate oxide and increases the collector-emitter saturation voltage $V_{CE,sat}$ and, consequently, the on-state losses. Alternatively, the reverse recovery peak can be reduced by decreasing the implantation dose of the anti-latch p^{++} emitter region. This method does not affect $V_{CE,sat}$, as do the above-mentioned methods. However, a reduction of this doping dose is limited by the over-current turn-off robustness (latch-up robustness).

The reverse recovery current of the RC-IGBT can also be reduced by applying a positive gate-emitter voltage for a short period of time (electronic realization). When the RC-IGBT operates in diode mode with a high and positive v_{GE}, a MOS-channel is created in the p^+ layer between the n^+ and the n^- layer. Therefore, hole injection is reduced, and as a result, the efficiency of the emitter p^+ layer is strongly decreased, as is the carrier density. In this way, a drastic reduction of the recovery charge can be achieved during the device turn-off transient [6, 47, 48].

As presented in [12], when the RC-IGBT is in reverse conduction mode, the number of charge carriers can be reduced by applying a positive gate-emitter voltage (desaturation pulse), leaving enough blanking time before the complementary RC-IGBT starts conducting. Although the switching losses are reduced, they are not minimized with this solution. The reason for this is that the MOS-channel should ideally be maintained, by means of the desaturation pulse, until a short time (e.g.100 ns) before the zero crossing of the current through the RC-IGBT operated in the diode mode, as presented in Sec. 4.3.2.

To overcome the problems described above, a novel scheme has been developed. The scheme includes the generation of a trigger pulse to reduce the switching losses and to ensure safe operation of the RC-IGBT. In addition, a method to automatically find the optimal parameters of the desaturation pulse (referred to here as "pre-trigger pulse") has been developed by means of a simple current detection technique. With this scheme, the reverse recovery current and the reverse recovery switching losses are minimized. Moreover, all these benefits are achieved without expensive and/or bulky components.

4.2 SWITCHING PARAMETERS OF RC-IGBTS

In this section the definitions of the parameters with the strongest influence on the switching behaviour of the RC-IGBT are presented.

Standard IGBT technology has been vastly investigated and improved. For example, in the latest generation of IGBTs the switching and conduction losses are reduced [49, 50] and external gate resistors can be almost eliminated ($R_G \approx 1\,\Omega$) [51].

As described in the previous section, the switching behaviour of the RC-IGBT in the diode mode can be improved by applying a short positive gate-emitter voltage just prior to the diode turn-off transient. This pre-trigger pulse (PT pulse) influences the effective emitter efficiency and, as a result, the reverse recovery current is reduced.

Fig. 4.2 shows fundamental waveforms of collector currents and trigger pulses with the inclusion of the PT pulse. In the example, the high-side RC-IGBT T_1 acts as a diode and the low-side RC-IGBT T_2 acts as an IGBT. Therefore, the PT pulse is only applied to T_1 by the signal s_1. It is turned on at t_0 and at t_1 the RC-IGBT T_2 is turned on by the signal s_2. The PT pulse ends at t_2. The overlapping time of s_1 and s_2 is named *delay time* $t_d = t_2 - t_1$; the time interval where the PT pulse is applied is named *PT pulse length* $t_{PT} = t_2 - t_0$. The instant when the gate-emitter voltage $v_{GE,RC1}$ during the turn-off transient of the PT pulse falls below the threshold voltage $V_{GE,th,RC}$ is defined as $t_{GC,RC}$. The instant of the zero crossing of the current of T_1 $i_{D,RC1}$ is defined as t_{zc}.

In the next section, the influence of the parameters t_d and t_{PT} on the switching losses of the RC-IGBT as well as the influence of the gate turn-off resistance $R_{G,OFF,D}$ of the PT pulse are investigated.

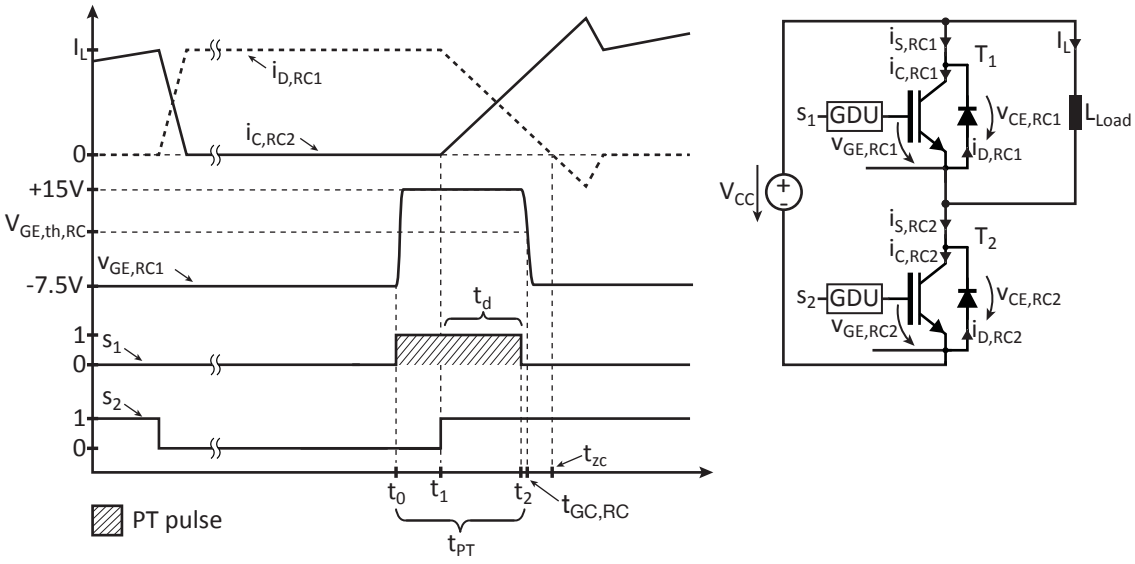


Figure 4.2: Fundamental waveforms of the collector currents and trigger signals with the pre-trigger pulse (PT pulse).

4.3 INVESTIGATION OF THE INFLUENCE OF THE SWITCHING PARAMETERS ON THE RC-IGBT

The influence of the parameters delay time t_d, length of the PT pulse t_{PT} and the gate turn-off resistance $R_{G,OFF,D}$ of the PT pulse on the switching losses of the RC-IGBT (200 A / 1200 V) were experimentally tested. This section presents the results and the description of the experimental tests.

4.3.1 Description of the experimental setup

The experimental investigation was carried out by applying a double pulse pattern to a buck converter with an inductive load. The double pulse test was described in Sec. 3.2.2. Two setup configuration were used: an IGBT (T_2) – RC-IGBT (T_1) configuration and an IGBT (T_2) – diode (D_1) configuration, as shown in Fig. 4.3a and Fig. 4.3b, respectively. The RC-IGBT operates in diode mode throughout the entire test in order to investigate the peak variation of the reverse recovery current ($I_{RR,D,RC}$). These results are compared with the results obtained with the IGBT configuration with a separate silicon (Si) diode (200 A / 1200 V) at different T_j values. The test bench is shown in Fig. 4.3c and a thermogram of the system operating at 124 °C is shown in Fig. 4.3d. The test conditions and the measurement instruments are described in Table 4.2. The RC-IGBT is commanded with a standard GDU which turns on the RC-IGBT with an on-state gate-emitter voltage V_{GEon} of +15 V and turns it off with an off-state gate-emitter voltage V_{GEoff} of −7.5 V.

Table 4.2: Test conditions for the investigation of the influence of the switching parameters on the RC-IGBT

Component / Instrument	Value	Description
C	6600 µF	DC-Link
L	76 µH	Inductive Load
RC-IGBT (T_1)	-	RC-IGBT (200 A/1200 V)
IGBT (T_2)	FF650R17IE4	IGBT (650 A/1700 V)
Oscilloscope	WaveSurfer 24xs	2.5 Gs/s, 200 MHz
Oscilloscope	WaveRunner 44xi	5 Gs/s, 400 MHz
Current probes	PEM CWT 6B	1.2 kA, 16 MHz
Voltage probes	Testec TT-SI 9110	1.4 kV, 100 MHz

4.3.2 Influence of the delay time t_d of the pre-trigger pulse on the switching losses

This section presents the experimental results of how the delay time t_d influences the switching losses of an RC-IGBT operated in diode mode. An optimal delay time $t_{d,opt}$ is defined as the time t_d that minimizes the switching losses of the RC-IGBT in diode mode. The test conditions are described in Table 4.3.

The current through the RC-IGBT in diode mode is defined as $i_{D,RC}$ and the reverse recovery peak current is defined as $I_{RR,D,RC}$. The IGBT collector current is $i_{C,T}$. The RC-IGBT collector-emitter voltage is defined as $v_{CE,RC}$ and the gate-emitter voltage as $v_{GE,RC}$. The turn-on losses of the IGBT are defined as $W_{ON,T}$ and the turn-off losses as $W_{OFF,T}$. The turn-on losses of the RC-IGBT operated as an IGBT are defined as $W_{ON,RC}$ and the turn-off losses as $W_{OFF,RC}$. When

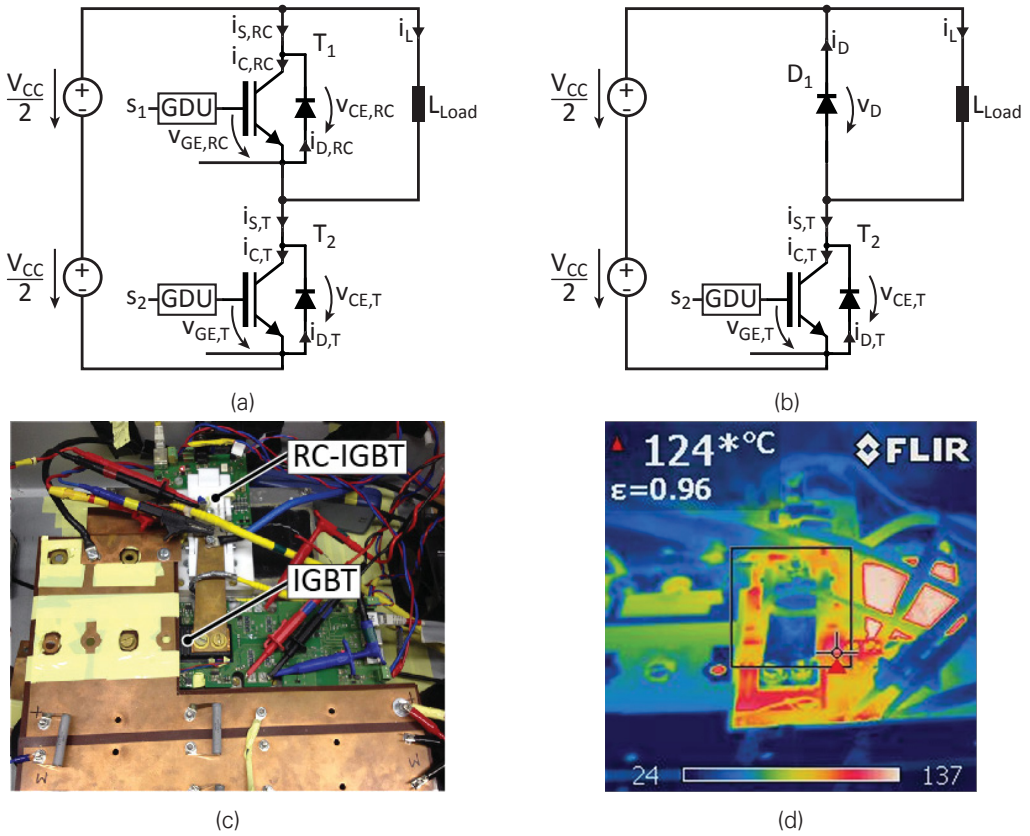


Figure 4.3: Test setup for the investigation of the influence of the switching behaviour of the RC-IGBT. (a) Setup topology RC-IGBT - IGBT configuration, (b) setup topology Diode - IGBT configuration, (c) experimental setup, and (d) thermogram at 124 °C.

Table 4.3: Test conditions for the investigation of the influence of t_d on the switching losses

Variable	Description
V_{CC}	100, 300 and 500 V
I_C	50...200 A
T_j	25, 75 and 125 °C
t_{PT}	2.5, 5, 8 and 10 µs

the RC-IGBT operates in diode mode, the turn-off losses are defined as $W_{OFF,D,RC}$. The turn-off losses of a conventional diode are defined as $W_{OFF,D}$.

Experimental results of the influence of the delay time t_d on the switching losses are presented in Fig. 4.4. Here the collector currents, collector-emitter voltages, switching losses, gate-emitter voltages and the input signals of the GDU (s_1 and s_2) are shown. Three cases are presented: an IGBT - diode configuration, an IGBT - RC-IGBT (in diode mode) without PT pulse and with a PT pulse with the optimal delay $t_{d,opt}$. When the PT pulse with $t_{d,opt}$ is applied, the switching losses are reduced by 35% in the IGBT and by 62% in the RC-IGBT in comparison to an RC-IGBT without PT pulse. In comparison to the losses of a IGBT configuration with a separate diode (200 A / 1200 V), the switching losses are reduced by 12% in the IGBT and by 40% in the RC-IGBT in diode mode.

The influence of different delay time t_d values on the behaviour of the RC-IGBT operated in diode mode were investigated, and the results are shown in Fig. 4.5. The delay time t_d is modified as $t_d = t_{d,opt} + t_{dx}$, where t_{dx}= +40, −40, −120, −200 and −400 ns. The figure shows the collector

current i_C and the collector-emitter voltages v_{CE} at the IGBT, the current $i_{D,RC}$ and voltage $v_{CE,RC}$ at the RC-IGBT, the turn-on switching losses of the IGBT ($W_{ON,T}$) and the turn-off switching losses of the RC-IGBT ($W_{OFF,D,RC}$), the gate-emitter voltages of the IGBT v_{GE} and RC-IGBT $v_{GE,RC}$, and the input signals of the GDU for the IGBT (s_2) and for the RC-IGBT (s_1).

When $t_d = t_{d,opt} - 400\,\text{ns}$, the switching losses are increased by 30% in the IGBT and by 35% in the RC-IGBT compared to the losses when $t_d = t_{d,opt}$. When $t_d = t_{d,opt} + 40\,\text{ns}$, the switching losses are increased by 3.2% in the IGBT and by 7.6% in the RC-IGBT.

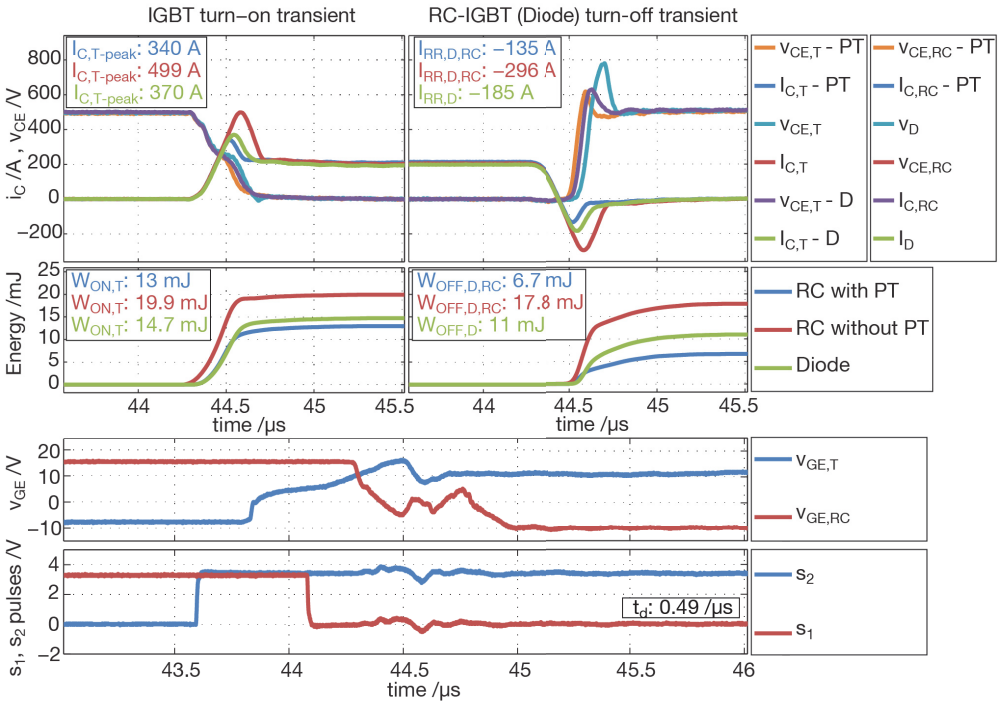


Figure 4.4: Waveform comparison of a diode, RC-IGBT without PT pulse and with PT pulse if an optimal t_d is used ($V_{CC} = 500\,\text{V}$, $I_C = 200\,\text{A}$, $T_j = 125\,°\text{C}$, $t_{PT} = 10\,\mu\text{s}$, $R_{G,OFF,D} = 1.18\,\Omega$).

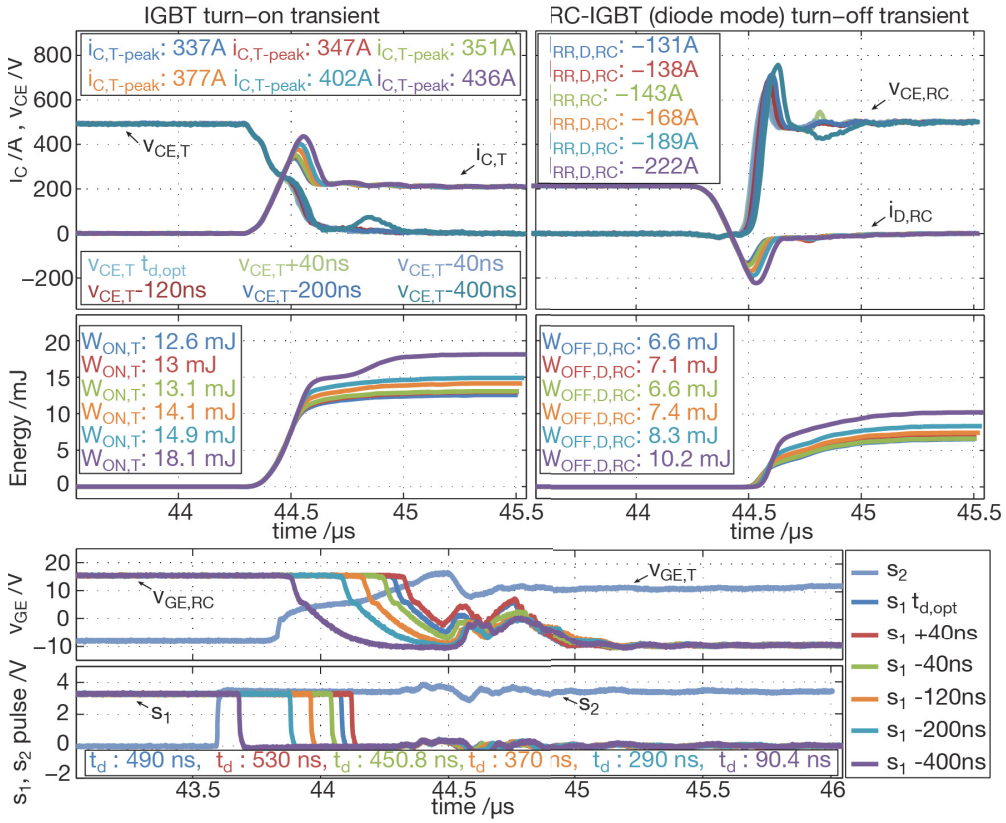


Figure 4.5: Waveforms of IGBT and RC-IGBT at different delay times t_d (V_{CC} = 500 V, I_C = 200 A, T_j = 125 °C, t_{PT} = 8 µs, $R_{G,OFF,D}$ = 1.18 Ω).

Theoretically, the optimal delay time $t_{d,opt}$ should occur when the RC-IGBT MOS-channel first becomes conductive, created by a positive gate-emitter voltage $v_{GE,RC}$, up until the zero crossing of the current $i_{D,RC}$. This is achieved by reducing the voltage $v_{GE,RC}$ at the device terminals below the threshold voltage (e.g. $V_{GE,th,RC} < 5.5$ V for the investigated RC-IGBT) t_x ns (e.g. t_x = 100 ns) before the zero crossing of the current $i_{D,RC}$. The time t_x depends on device internal processes and the delay introduced by the passive low pass filter formed by the external and the internal gate resistances as well as the internal capacitance C_{GE} of the RC-IGBT.

The current $i_{D,RC}$ during the reverse recovery process of the RC-IGBT at different time delay t_d values for $I_{D,RC}$ of 150 A and 200 A are presented in Fig. 4.6 and in Fig. 4.7 respectively. The moment of the current zero crossing and the moment when $v_{GE,RC}$ falls below its threshold voltage $V_{GE,th,RC}$ for the optimal time delay are marked with a dotted line. For both examples, the optimal time delay $t_{d,opt}$ is achieved when the MOS-channel is turned off ($v_{GE,RC} < V_{GE,th,RC}$) around 100 ns before the zero crossing of the current $i_{D,RC}$ ($t_{zc} - t_{GC,RC} \approx 100$ ns).

The variation of the RC-IGBT reverse recovery peak current ($I_{RR,D,RC}$) at different delay time t_d values for a current $I_{D,RC}$ of 200 A is shown in Fig. 4.8. The lowest reverse recovery peak $I_{RR,D,RC}$ is achieved when the delay time is around $t_d = t_{d,opt}$ = 490 ns. The influence of the time difference between the moment of the zero crossing of the current $i_{D,RC}$ t_{zc} and the moment of the closing of MOS-channel $t_{GC,RC}$ ($t_{zc} - t_{GC,RC}$) on the reverse recovery peak current $I_{RR,D,RC}$ is presented in Fig. 4.9. The figure presents the result at three different operating current $I_{D,RC}$ values. In all the tests, the lowest reverse recovery peak current $I_{RR,D,RC}$ is achieved when $t_{zc} - t_{GC,RC} \approx 100$ ns.

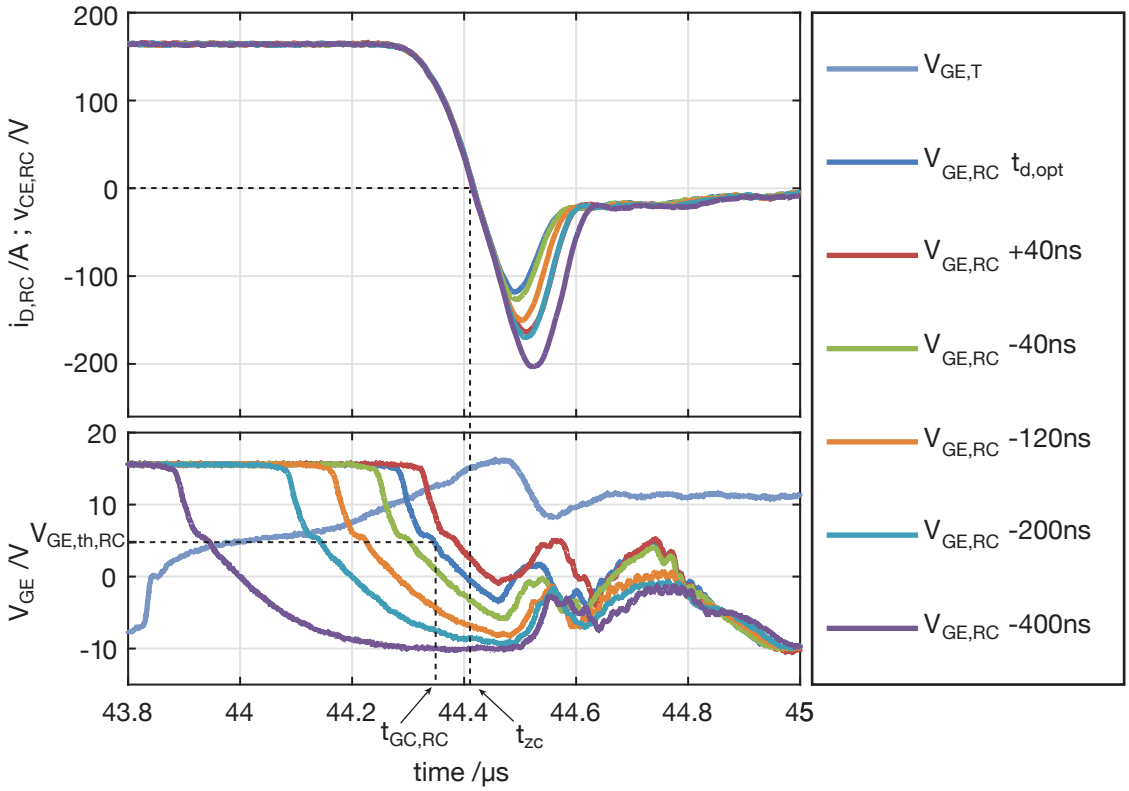


Figure 4.6: Reverse recovery current at different delay times t_d (V_{CC} = 500 V, $I_{D,RC}$ = 150 A, T_j = 125 °C, t_{PT} = 8 µs, $R_{G,OFF,D}$ = 1.18 Ω).

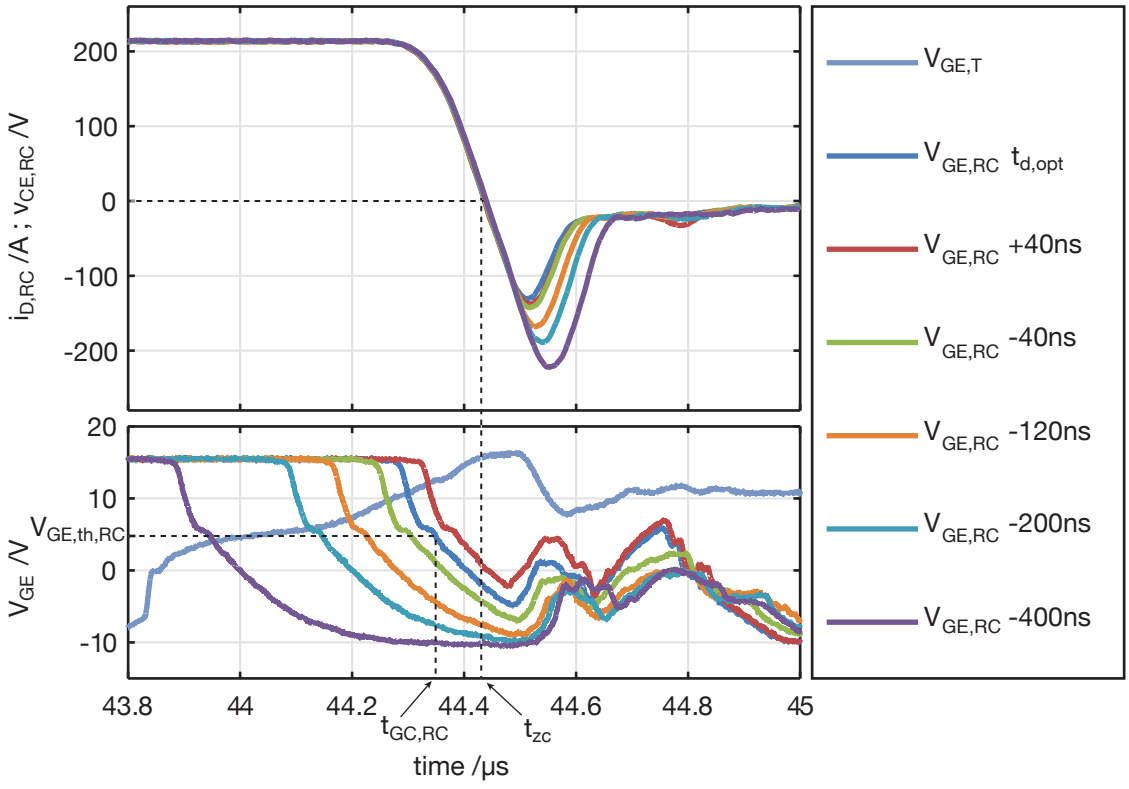


Figure 4.7: Reverse recovery current at different delay times t_d (V_{CC} = 500 V, $I_{D,RC}$ = 200 A, T_j = 125 °C, t_{PT} = 8 µs, $R_{G,OFF,D}$ = 1.18 Ω).

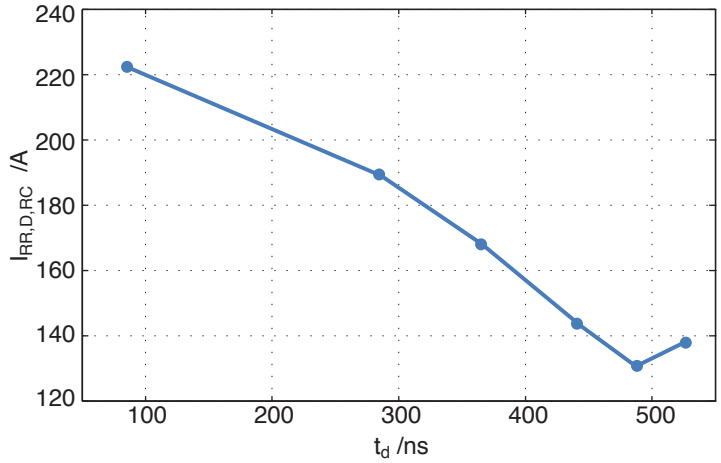


Figure 4.8: Reverse recovery current peak of the RC-IGBT at different delay times t_d (V_{CC} = 500 V, $I_{D,RC}$ = 200 A, T_j = 125 °C, t_{PT} = 8 µs, $R_{G,OFF,D}$ = 1.18 Ω).

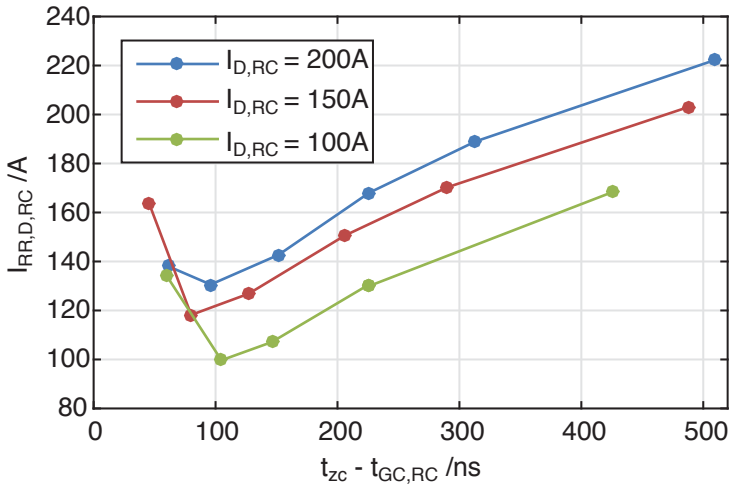


Figure 4.9: Reverse recovery current peak of the RC-IGBT at different delay times t_d respect to $t_{zc} - t_{GC,RC}$ (V_{CC} = 500 V, T_j = 125 °C, t_{PT} = 8 µs, $R_{G,OFF,D}$ = 1.18 Ω).

A summary of the experimental results is shown in Fig. 4.10, where the dependency of $t_{d,opt}$ regarding the collector current, V_{CC} and T_j is depicted. This information is important for the concept of the GDU of RC-IGBTs in voltage source converters. The optimal time point to decrease the gate-emitter voltage below the threshold voltage is slightly before the zero crossing of the current of the RC-IGBT in diode mode. Therefore, $t_{d,opt}$ depends on the diode current before the commutation and the occurring *di/dt* during the commutation. The experimental results in Fig. 4.10 show that $t_{d,opt}$ is linearly dependent on the collector current and junction temperature at low DC-link voltage V_{CC} = 100 V (blue lines). In detail, $t_{d,opt}$ varies from 600 to 750 ns for $i_{D,RC}$ between 100 and 200 A.

However, at V_{CC} over 300 V this dependency is not so strong. For example, when V_{CC} is 500 V (green lines), $t_{d,opt}$ varies by 50 ns (from 450 to 500 ns) throughout the entire current range and it is only weakly temperature-dependent. Therefore, $t_{d,opt}$ could be chosen to remain constant during the entire current range operation of the RC-IGBT in a converter operating with a DC-link voltage V_{CC} above 500 V.

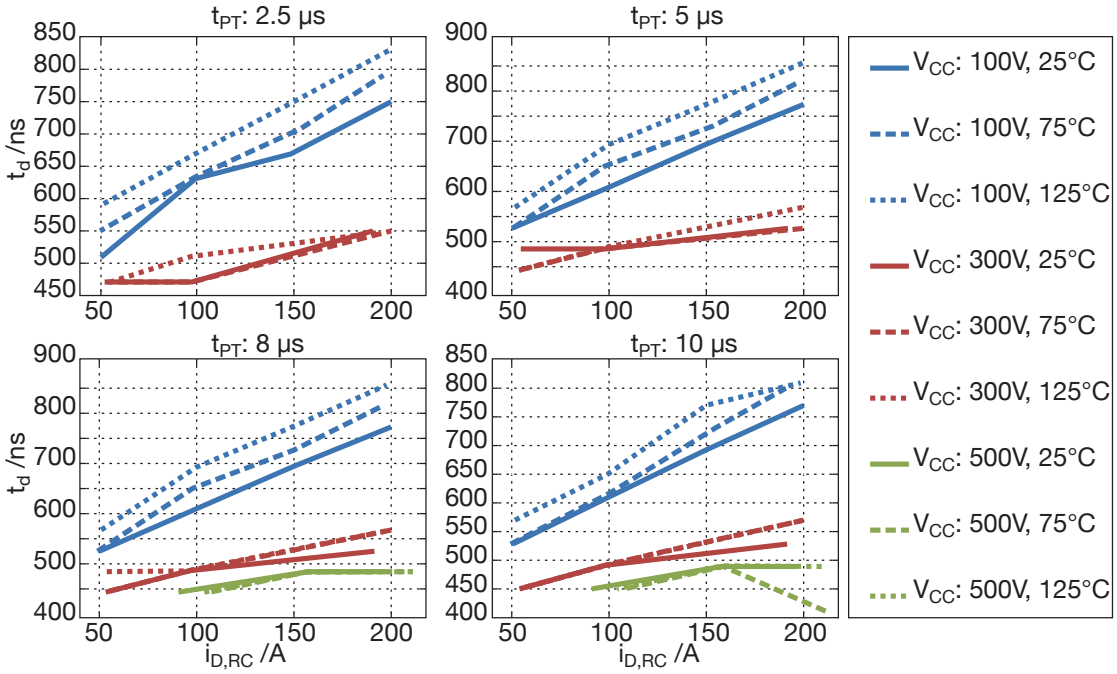


Figure 4.10: Optimal delay vs. collector current at different V_{CC}, I_C and T_j values.

4.3.3 Influence of pre-trigger pulse length t_{PT} on the switching losses

This section presents the results of the experimental investigation of the influence of the length of the PT pulse t_{PT} on the turn-off behaviour of the RC-IGBT in diode mode. During the tests, the length of the PT pulse t_{PT} is modified, while the delay time t_d is kept constant at the optimal delay time $t_d = t_{d,opt}$. The test conditions are listed in Table 4.4.

The length of the PT pulse t_{PT} is adjusted from 0.5 µs to 2.5 µs with a fixed delay time $t_d = t_{d,opt}$ = 490 ns. The influence of the pulse length t_{PT} on turn-off losses of the RC-IGBT in diode mode $W_{OFF,D,RC}$ is presented in Fig. 4.11. When t_{PT} increases from 0.5 µs to 1.5 µs the turn-off losses $W_{OFF,D,RC}$ decrease from 3.3 mJ to 2 mJ. Fig. 4.12 shows the turn-off losses as a function of t_{PT} ($W_{OFF,D,RC} = f(t_{PT})$). The turn-off losses $W_{OFF,D,RC}$ are reduced by 60% for a t_{PT} greater than 1.5 µs. These results indicate that there is a minimum pulse length to achieve a minimum

Table 4.4: Test conditions for the investigation of the influence of the PT pulse length on the switching losses

Variable	Description
V_{CC}	100, 300 and 500 V
I_C	50...200 A
T_j	25 °C
t_{PT}	0.5...2.5 µs
t_d	$t_{d,opt}$ = 490 ns

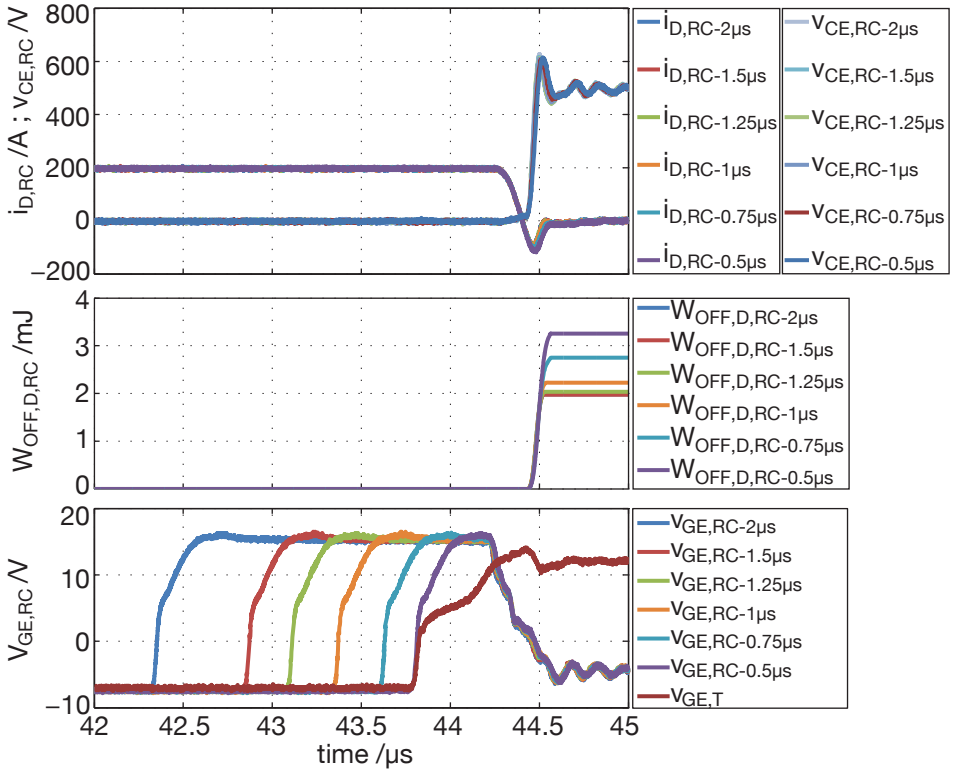


Figure 4.11: Influences of different t_{PT} values on the switching losses of the RC-IGBT (V_{CC} = 500 V, I_C = 200 A and T_j = 25 °C).

reverse recovery charge for given operating conditions. A further increase of the pulse length $t_{PT} > 1.5$ µs does not cause a further decrease of the corresponding turn-off losses $W_{OFF,D,RC}$. The required pulse length to achieve a minimum turn-off losses ($t_{PT} \geq 1.5$ µs) means that the pre-trigger pulse (PT pulse) must be initiated before (e.g. 1.1µs in Fig. 4.11) the turn-on transient of the corresponding IGBT.

4.3.4 Influence of the gate turn-off resistance $R_{G,OFF,D}$ of the turn-off transient of the pre-trigger pulse on the switching losses

The influence of the value of the gate turn-off resistance $R_{G,OFF,D}$ on the switching losses of the RC-IGBT in diode mode was experimentally investigated. The delay time t_d and the PT pulse length t_{PT} were held constant during the test. The gate turn-off resistance value was manually modified on the GDU. The test conditions are listed in Table 4.5.

Throughout the test, the PT pulse was applied with an optimal delay time $t_{d,opt}$ = 490 ns and a t_{PT} equal to 8 µs. The PT pulse is turned off with different gate turn-off resistance values $R_{G,OFF,D}$.

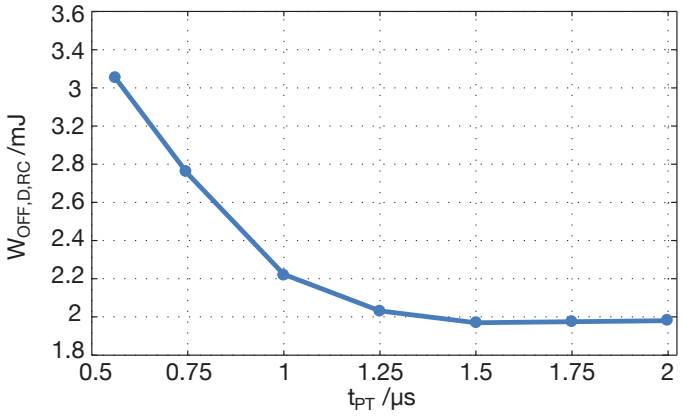


Figure 4.12: Relation between the length of the PT pulse t_{PT} and the RC-IGBT switching losses (V_{CC} = 500 V, I_C = 200 A and T_j = 25 °C).

Table 4.5: Test conditions for the investigation of the influence of $R_{G,OFF,D}$ on switching losses

Variable	Description
V_{CC}	100, 300 and 500 V
I_C	50...200 A
T_j	25 °C
t_{PT}	8 µs
$R_{G,OFF,D}$	5.5 and 1.1 Ω
t_d	$t_{d,opt}$ = 490 ns

The influence of $R_{G,OFF,D}$ on the turn-on switching losses of the complementary IGBT $W_{ON,T}$ is presented in Fig. 4.13. The blue and red lines represent the switching losses when the PT pulse, applied to the RC-IGBT, is turned off with $R_{G,OFF,D}$ of 5.5 and 1.1 Ω respectively. The green line represents the switching losses when the PT pulse is not applied. The orange dotted line represents the switching losses when a conventional diode is used instead of an RC-IGBT. With an $R_{G,OFF,D}$ of 5.5 Ω the switching losses are similar to the switching losses of an IGBT working with a conventional diode. If an $R_{G,OFF,D}$ of 1.1 Ω is used in the RC-IGBT instead, the turn-on losses of the IGBT are reduced by 26.5%.

The turn-off losses of the RC-IGBT operated in diode mode $W_{OFF,D,RC}$ are presented in Fig. 4.14. With an $R_{G,OFF,D}$ of 5.5 Ω the turn-off losses $W_{OFF,D,RC}$ are 56 % higher than the turn-off losses of a conventional diode in an IGBT – diode configuration (V_{CC} = 500 V Fig. 4.14). When $R_{G,OFF,D}$ is 1.1 Ω the losses of the RC-IGBT are 25% lower than the turn-off losses of a conventional diode in an IGBT – diode configuration (V_{CC} = 500 V, Fig. 4.14).

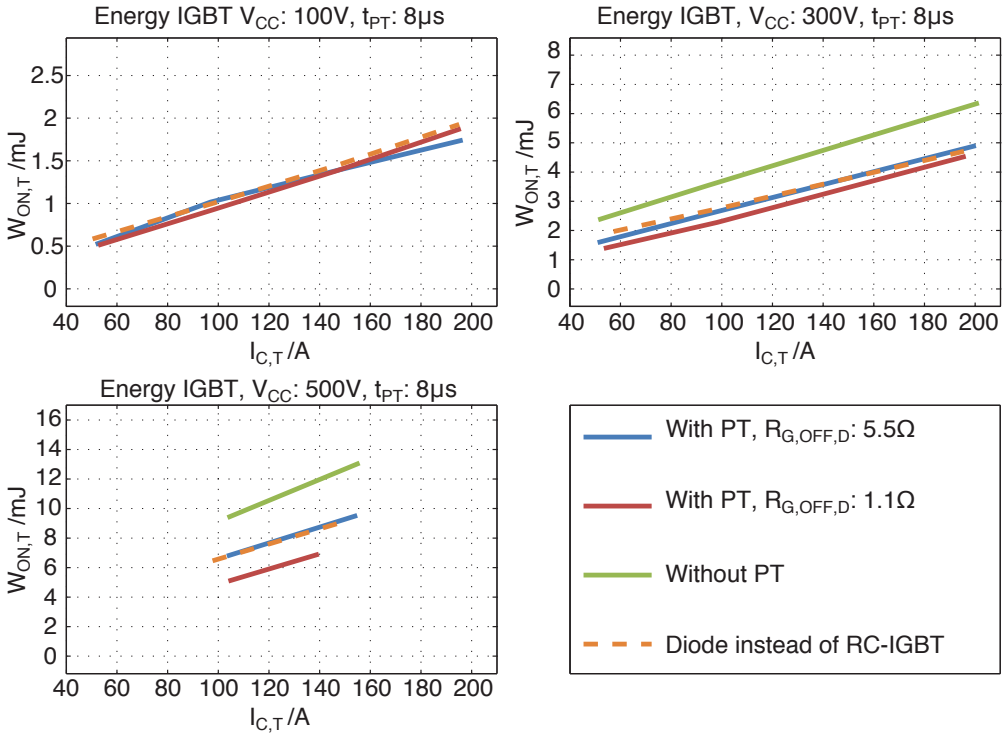


Figure 4.13: Turn-on switching losses of the IGBT at different $R_{G,OFF,D}$ resistance values (T_j = 25 °C).

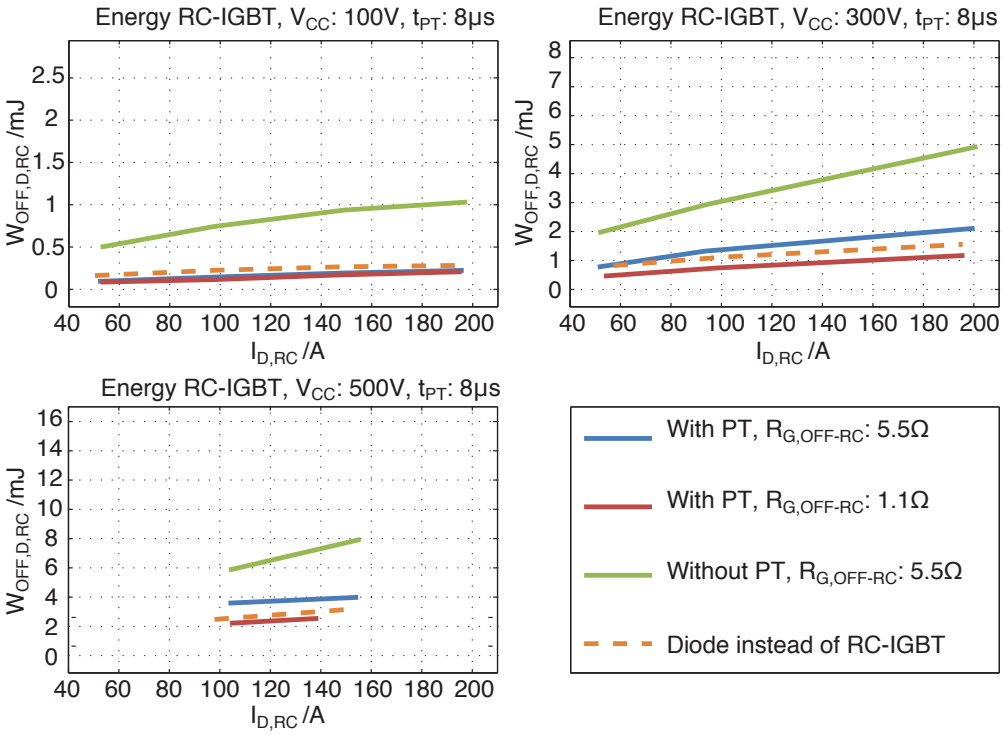


Figure 4.14: Turn-off switching losses of the RC-IGBT at different $R_{G,OFF,D}$ resistance values (T_j = 25 °C).

4.3.5 Summary of the results

According to the experimental results, the following parameters influence the switching behaviour of the RC-IGBT in diode mode:

- **Pre-trigger pulse (PT pulse):** The application of a PT pulse strongly reduces the reverse recovery peak current and consequently the turn-off switching losses of the RC-IGBT when it is applied with optimal time delay $t_{d,opt}$ and pulse length.
- **Optimal delay time ($t_{d,opt}$):** The application of a PT pulse with optimal delay time enables a reduction of the turn-off switching losses by e.g. 60% in an RC-IGBT compared to an RC-IGBT without PT pulse. The optimal delay time $t_{d,opt}$ is almost independent of the collector current and the junction temperature T_j for DC-link voltages V_{CC} greater than 500 V. Therefore, an optimal delay time $t_{d,opt}$ can be determined at one collector current level and this delay time can be applied for a larger current range. However, a deviation of ± 40 ns from $t_{d,opt}$ causes an increment of the switching losses by 7.6% in the RC-IGBT compared to the switching losses when $t_d = t_{d,opt}$ (V_{CC} = 500 V, I_C = 200 A, T_j = 125 °C, t_{PT} = 8 µs and $R_{G,OFF,D}$ = 1.18 Ω). For the investigated RC-IGBT, the optimal delay is achieved when the PT pulse is terminated ($v_{GE,RC} \leq V_{GE,th,RC}$) around 100 ns before the zero crossing of the current $i_{D,RC}$ to achieve minimum switching losses in the turning on IGBT and the turning off RC-IGBT operated as a diode.
- **Pre-trigger pulse length (t_{PT}):** For the RC-IGBT being investigated the pre-trigger pulse length should exceed about 1.5 µs ($t_{PT} \geq 1.5$ µs).
- **Gate turn-off resistances ($R_{G,OFF}$ and $R_{G,OFF,D}$):** The RC-IGBT should be operated with two different gate turn-off resistance values. If the RC-IGBT is operated as an IGBT and turned off, the corresponding gate resistance $R_{G,OFF}$ should be designed as would be a conventional IGBT considering e.g. over-voltages, SOA, *dv/dt*, *di/dt* and switching losses.

  If the RC-IGBT is operated as a diode the corresponding gate resistance to terminate the pre-trigger pulse (PT pulse) can be chosen to be as small as possible to prevent undesired oscillations. A small gate resistance (e.g. $R_{G,OFF,D}$ = 1.1 Ω) discharges the input capacitances close to zero crossing of the collector current when a pre-trigger pulse (PT pulse) with the optimum delay time $t_{d,opt}$ is applied.

4.4 AUTOMATIC DETERMINATION OF THE OPTIMAL DELAY

In the previous section, the influence of different parameters on the switching behaviour and losses of the RC-IGBT were investigated and explained. The most critical parameter is the delay time t_d. An improper delay time t_d will cause an increase of the switching losses of the RC-IGBT operated as a diode and can even cause a short circuit.

The delay time t_d has a dependency on the current through the RC-IGBT in diode mode $i_{D,RC}$, since the MOS-channel should be closed some nanoseconds before $i_{D,RC}$ = 0 A during inductive commutations. However, for high DC-Link voltages V_{CC} (e.g. $V_{CC} > 500$ V) this dependency decreases. In the previous section, $t_{d,opt}$ has been found manually. However, in an industrial implementation, it would be a major advantage if it could be determined automatically. Therefore, in the following, a scheme that achieves this purpose is presented.

The automatic determination of $t_{d,opt}$ is based on a measurement of and decreasing the reverse recovery peak current $I_{RR,D,RC}$ of the RC-IGBT. This section explains the hardware and software implementation of this scheme.

4.4.1 Estimation of the collector current

In the proposed method the current through the RC-IGBT in diode mode $i_{D,RC}$ is estimated by using the *current estimation method by comparison* proposed in Section 3.1.2.

The principle of the current estimation method of a RC-IGBT is shown in Fig. 4.15. The voltage v_{bond} is sensed and compared with a low threshold value. A logic signal $v_{meas,i\text{-}off}$ is generated, where the pulse length $t_{meas,i\text{-}off}$ represents the period in which the reference voltage $V_{ref\text{-}off}$ has been exceeded. The time interval $t_{meas,i\text{-}off}$ is related to the sum of the on-state current through the RC-IGBT operated in diode mode $I_{D,RC}$ and the reverse recovery current $I_{RR,D,RC}$ ($I_{D,RC} + I_{RR,D,RC}$). This method enables a simple and fast estimation of the current during switching transients.

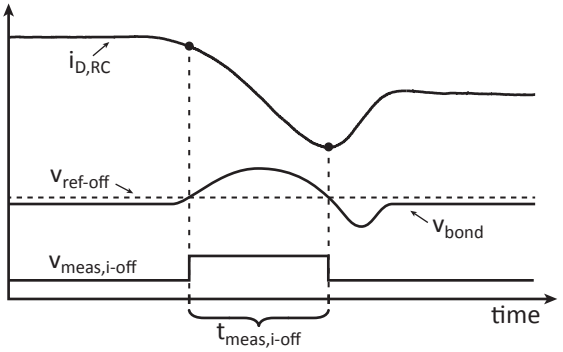


Figure 4.15: Example waveforms of the estimation of the RC-IGBT current.

4.4.2 Start-up routine to find the optimal delay time $t_{d,opt}$ automatically

This section presents an automatic calibration process to find the optimal delay time ($t_{d,opt}$). The algorithm applies a double pulse test (see Sec. 3.2.2) and a PT pulse. In every test, the algorithm estimates the $I_{D,RC} + I_{RR,D,RC}$ current and it modifies the delay time t_d value of the PT pulse for a given collector current. This test is repeated until the peak reverse recovery $I_{RR,D,RC}$ is minimized. One option for the implementation of this scheme in an industrial converter is the integration in a start-up routine of a converter.

A block diagram of the start-up routine is presented in Fig. 4.16. The software has been designed for a buck converter topology as presented in Fig. 4.2. The delay time t_d is adjusted in steps of 40 ns until the optimal delay time $t_{d,opt}$ has been found. The algorithm is divided in two sections, *initialization* and *loop*:

Initialization

1. **Initial delay $t_d = 0$:** The PT pulse of the RC-IGBT in the diode mode is terminated when the turn-on trigger pulse of the complementary RC-IGBT starts. A short circuit situation is avoided.
2. **Pulse_pattern is applied:** A double pulse test including a PT pulse for the RC-IGBT acting as a diode is applied.
3. **$t_{meas,i\text{-}off}$ is acquired:** This value is assigned to the variable m_1.

Loop

4. $\boldsymbol{t_d = t_d + k \cdot \Delta t}$ **:** The delay time t_d is incremented in steps Δt of 40 ns. The variable k is a positive scale factor in order to accelerate the finding of the optimal delay time $t_{d,opt}$.
5. $\boldsymbol{k = k - 1}$**:** The variable k is reduced each time the loop is repeated. Because $t_{meas,i\text{-}off}$ does not change considerably for a t_d below 80 ns, as the experimental data has shown, the minimum value of k is 2.
6. **Pulse_pattern is applied:** The double pulse test is repeated with the new delay time t_d.
7. $\boldsymbol{t_{meas,i\text{-}off}}$ **is acquired:** The new time interval $t_{meas,i\text{-}off}$ is acquired and assigned to the variable m_2. In every step that t_d gets closer to $t_{d,opt}$, the reverse recovery peak current $I_{RR,D,RC}$ as well as $t_{meas,i\text{-}off}$ are reduced.
8. $\boldsymbol{m_1}$ **is compared with** $\boldsymbol{m_2}$ **:**
   - **If** $\boldsymbol{m_2}$ **is equal or less than** $\boldsymbol{m_1}$, switch the variables $m_1 = m_2$ and repeat the process from the step 4.
   - **Else** $\boldsymbol{m_2}$ **is greater than** $\boldsymbol{m_1}$, the reverse recovery peak current $I_{RR,D,RC}$ has increased compared to the last step. Therefore, the optimal delay time $t_{d,opt}$ was found in the last step $\boldsymbol{t_{d,opt} = t_d - k \cdot \Delta t}$.

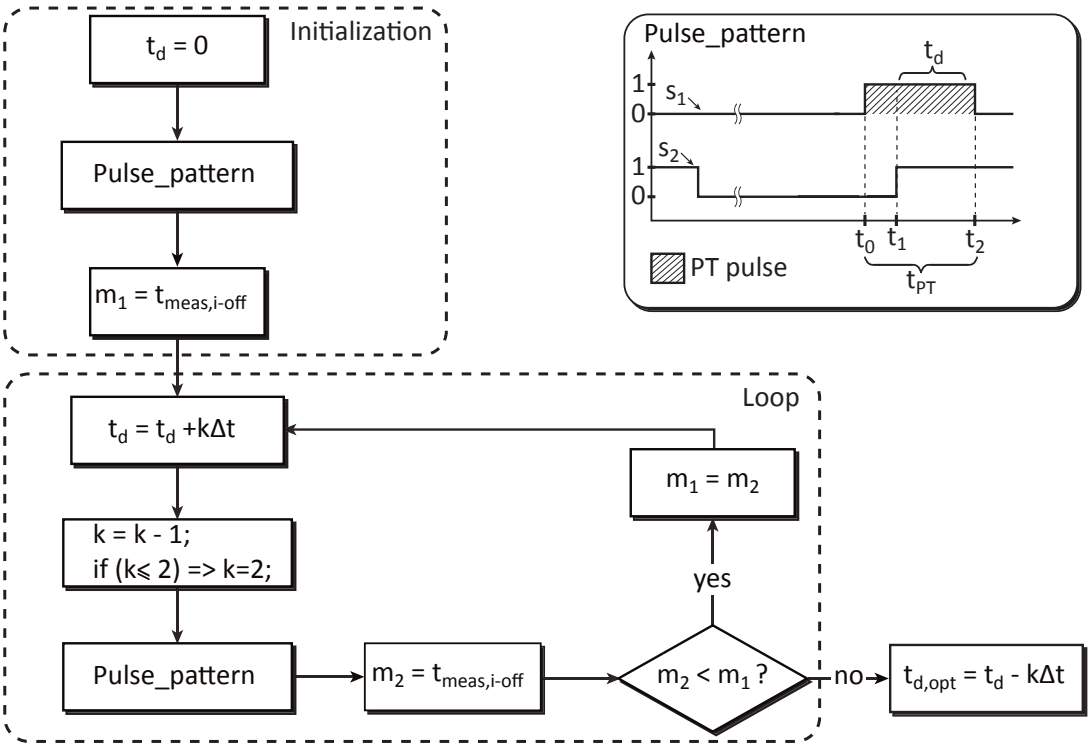


Figure 4.16: Block diagram of the automatic determination of the optimal delay $t_{d,opt}$ algorithm.

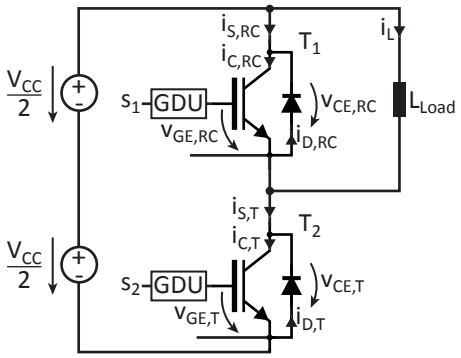
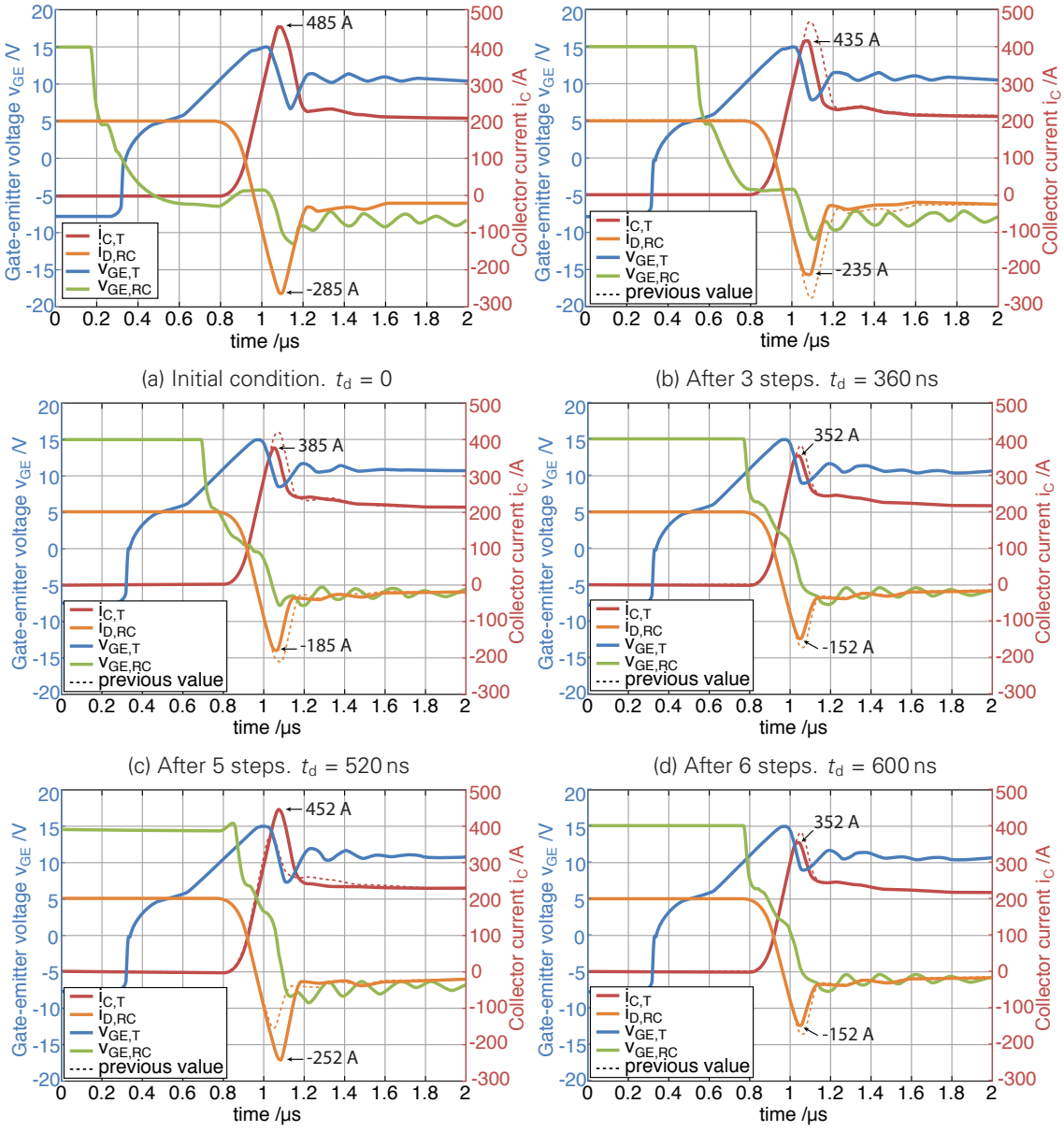


Figure 4.17: Setup topology for the verification of the algorithm to automatically determine $t_{d,opt}$.

The operation of the algorithm has been experimentally tested with one IGBT (T_2) and one RC-IGBT (T_1) operated in diode mode, as presented in Fig. 4.17. The optimal delay $t_{d,opt}$ is found for an on-state current through the RC-IGBT operated in diode mode $I_{D,RC}$ = 200 A and V_{CC} = 500 V. The pre-trigger pulse length t_{PT} is t_{PT} = 1.5 µs for the entire test.

Fig. 4.18 shows the operation of the automatic determination of $t_{d,opt}$. Each figure shows the turn-on transient of the IGBT and the turn-off transient of the RC-IGBT for a specific delay time t_d. The orange line represents the current through the RC-IGBT in diode mode $i_{D,RC}$. The red line represents the collector current $i_{C,T}$ of the IGBT. The blue line represents the gate-emitter voltage of the IGBT $v_{GE,T}$. The green line represents the gate-emitter voltage of the RC-IGBT $v_{GE,RC}$, where the termination of the PT pulse can be appreciated. The dotted lines represent the previous current waveforms.

Initially, with t_d = 0, the PT pulse is turned off at the same time as the digital signal turns on the IGBT. The peak current of T_2 $i_{C,T}$ is about 485 A. After three steps the time delay t_d is adjusted to 360 ns and the peak current of T_2 $i_{C,T}$ is reduced to 435 A. After five steps the time delay t_d is adjusted to 520 ns and the peak current of T_2 $i_{C,T}$ is reduced to 385 A. After six steps the system finds the optimal delay time, which is around $t_{d,opt}$ = 600 ns and the peak current of T_2 $i_{C,T}$ is about 352 A. The start-up routine applies one more step, the time delay t_d is increased to 680 ns and the peak current of T_2 $i_{C,T}$ raises up to approximately 452 A. Eventually, the algorithm detects a raise of the current and decreases the delay by 80 ns achieving $t_{d,opt}$ after eight steps. Thus the result of step 8 is equivalent to that of step 6.



(a) Initial condition. $t_d = 0$

(b) After 3 steps. $t_d = 360\,\text{ns}$

(c) After 5 steps. $t_d = 520\,\text{ns}$

(d) After 6 steps. $t_d = 600\,\text{ns}$

(e) After 7 steps. $t_d = 680\,\text{ns}$

(f) After 8 steps. The optimal delay was found one step backward (equivalent to step 6).

Figure 4.18: Verification of the operation of the start-up routine ($V_{CC} = 500\,\text{V}$, $I_{D,RC} = 200\,\text{A}$, $T_j = 25\,°\text{C}$, $R_{G,OFF,D} = 1.18\,\Omega$).

4.5 CONTROL SCHEME FOR A CONVERTER WITH SINUSOIDAL LOAD CURRENT

The application of RC-IGBTs in a voltage source converter features several advantages (see Section 4.1 pp. 50-51). The experimental investigations showed that, additionally, switching losses could be reduced if a suitable PT pulse is used. However, the incorrect application of PT pulse can increase the switching losses and can even lead to short circuits. This section presents a suitable scheme for pulse generation for a 2L-VSC converter with RC-IGBTs. Ideal waveforms of a standard PWM for a 2L-VSC converter with conventional IGBTs and diodes are presented in Fig. 4.19. The IGBT modulation signal s_1 is the inverse of the IGBT modulation signal s_2 ($s_1 = \overline{s_2}$). A delay

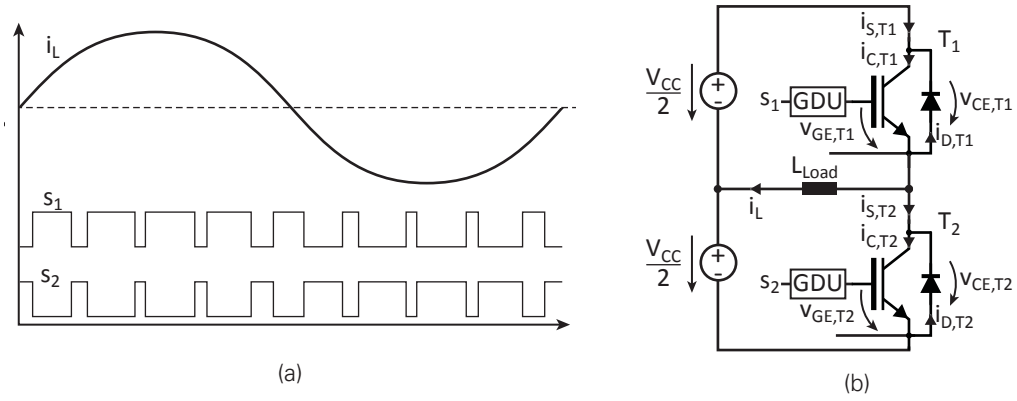


Figure 4.19: Ideal modulation signals and sinusoidal output current of a standard PWM waveforms of a 2L-VSC converter with conventional IGBTs/diodes. (a) PWM modulation signals, and (b) equivalent circuit for one phase of a 2L-VSC.

time between turn-off transients and turn-on transients is usually introduced to avoid dynamic short circuit currents during commutations in real converters (e.g. [52]).

When RC-IGBTs are used in a converter and they act as a diode, their trigger signals should only include the PT pulses. Thus the on-state voltage, and consequently, the on-state losses of the RC-IGBT are reduced [11, 44, 45]. Fig. 4.20 shows the diode on-state characteristic of the (200 A / 1200 V) RC-IGBT being considered. The on-state voltage of the RC-IGBT in diode mode ($v_f = -v_{CE,RC}$) is increased by 60% if a gate-emitter voltage $v_{GE,RC}$ of 15 V instead of −7.5 V is applied.

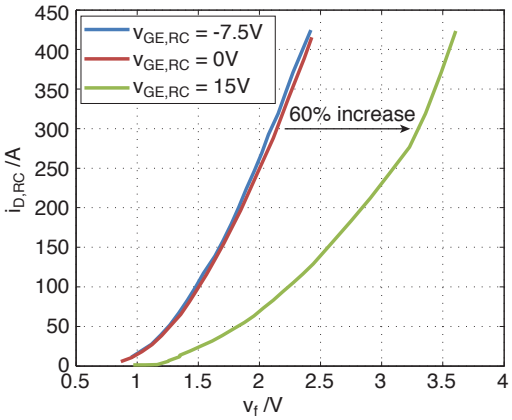


Figure 4.20: On-state voltage of the considered (200 A / 1200 V) RC-IGBT acting as a diode at different gate-emitter voltages v_{GE}. T_j = 25°C.

An example of the pulse modulation for the 2L-VSC converter with RC-IGBTs is shown in Fig. 4.21. If the load current i_L is positive, the RC-IGBT T_2 acts as a diode; if i_L is negative, the RC-IGBT T_1 acts as a diode. The pulse generation scheme must be able to:

- apply the PT pulse and to disable the conventional modulation signal when the RC-IGBT acts as a diode, and
- apply the PT pulse with a reduced gate turn-off resistance value.

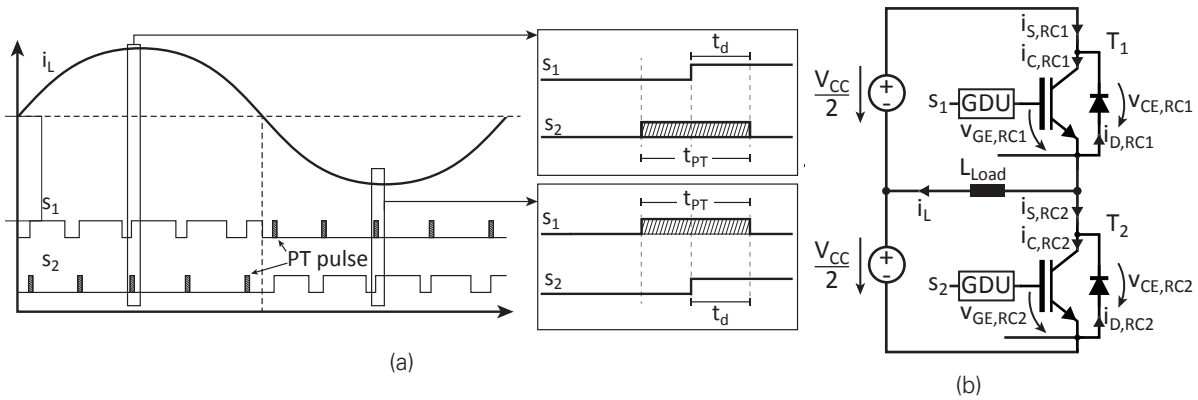


Figure 4.21: Ideal modulation signals and sinusoidal output current waveforms of a 2L-VSC converter with RC-IGBTs. (a) Modulation signals, and (b) equivalent circuit for one phase of a 2L-VSC.

Fig. 4.22 shows a concept diagram of the proposed scheme to generate the trigger pulses, where the following stages can be depicted:

- **Pulse generation:** This stage contains an algorithm in a digital platform (e.g. FPGA), which is used to obtain $t_{d,opt}$ automatically and to generate suitable trigger pulses for a 2L-VSC with RC-IGBTs.
- **Current estimation:** This stage estimates a time which is equivalent to the sum of the on-state current in the RC-IGBT in diode mode $I_{D,RC}$ and the reverse recovery peak current $I_{RR,D,RC}$ ($I_{D,RC}+I_{RR,D,RC}$) according to the method explained in Sections 3.1.2 and 4.4.1. This function is implemented in the GDU and it is used to determine $t_{d,opt}$ as explained in section 4.4.
- **v_{CE} measurement:** This stage is used to determine whether the RC-IGBT acts as a diode or as an IGBT. This function is implemented in the GDU.
- **Output stage with two gate turn-off resistances:** This stage is used to trigger the RC-IGBT with appropriate gate turn-off resistances. This function is implemented in the GDU.

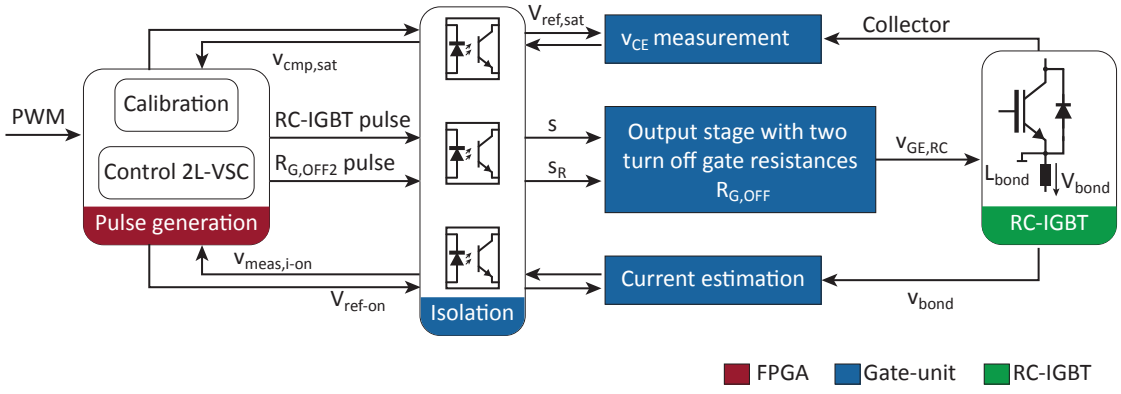


Figure 4.22: Block diagram of the trigger pulse generation for a 2L-VSC converter with RC-IGBTs.

4.5.1 Determination of the state of the RC-IGBT

The operation of a RC-IGBT with pre-trigger pulses when it acts as a diode requires a detection method to ascertain, if the RC-IGBT operates in IGBT or diode mode (see Fig. 4.21). In the proposed scheme, the state of the RC-IGBT (diode or IGBT) is determined by measuring the collector-emitter voltage $v_{CE,RC}$ of the RC-IGBT, similar to the method presented in Section 2.6.2.1. If the RC-IGBT acts as a diode and carries current (e.g. $i_{D,RC} = -i_{S,RC} > 0$), the voltage $v_{CE,RC}$ is equivalent to the negative value of the on-state voltage of a diode v_f (e.g. $v_{CE,RC} = -v_f \approx -2\,\text{V}$). If the RC-IGBT acts as an IGBT in on-state mode, the current $i_{S,RC}$ is positive (e.g. $i_{C,RC} = i_{S,RC} > 0$) and $v_{CE,RC}$ is equivalent to the saturation voltage of an IGBT $V_{CE,sat}$ which is a small positive value (e.g. $v_{CE,RC} = V_{CE,sat} \approx +3\,\text{V}$).

The implementation of the detection scheme is presented in Fig. 4.23. The collector-emitter voltage of the RC-IGBT $v_{CE,RC}$ is sensed through the diode D_1 and the voltage, $v_{CEm,sat}$, is compared with a small reference voltage $V_{ref,sat}$ close to 0 V. The output signal of the comparator is sent to the FPGA as an isolated digital signal $v_{cmp,sat}$, which is an indicator of the state of the RC-IGBT in the on-state mode (IGBT or diode mode). A logical "1" of $v_{cmp,sat}$ indicates that the RC-IGBT acts as an IGBT. Thus the PWM signal is applied and the PT pulse is disabled. On the contrary, a logical zero of $v_{cmp,sat}$ indicates that the RC-IGBT acts as a diode. Thus the PT pulse is applied and the PWM signal is disabled.

The measurement of the collector-emitter voltage as a polarity change of the collector current through the RC-IGBT $i_{S,RC}$ is presented in Fig. 4.24. This figure shows collector currents at two different di_C/dt and the respective collector-emitter voltages. During the zero crossing of the current, the collector-emitter voltage changes its polarity.

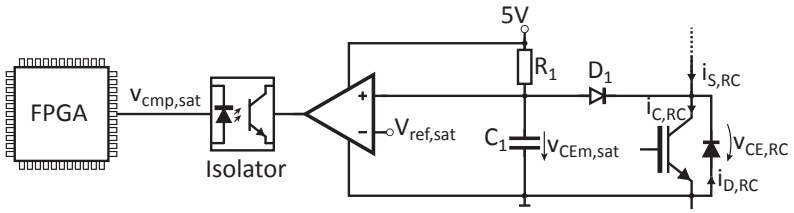


Figure 4.23: Proposed scheme for the detection of the on-state current $i_{S,RC}$ direction in an RC-IGBT.

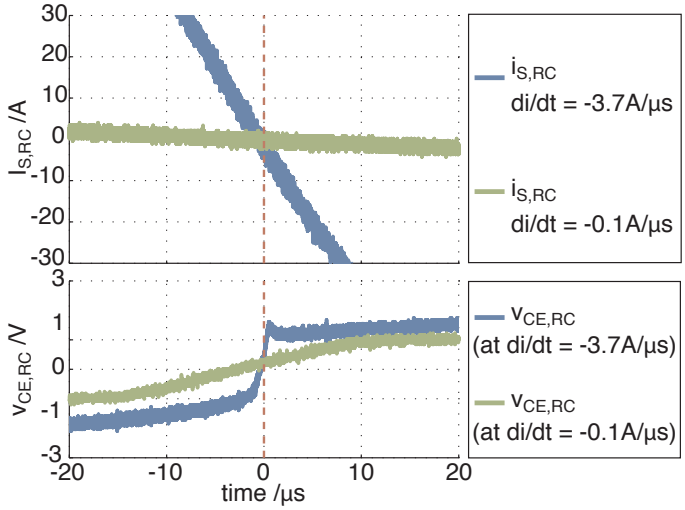


Figure 4.24: Collector-emitter voltage $v_{CE,RC}$ during an on-state zero-crossing current of $i_{S,RC}$ at two different di/dt values ($T_j = 25\,°\text{C}$).

4.5.2 Selection of a reduced gate turn-off resistance *(Output stage with two gate turn-off resistances)*

The output stage is used to charge and to discharge the input capacitances of the RC-IGBT in order to turn it on or off. The RC-IGBT is driven by an output stage with BJTs and two different gate turn-off resistances, as shown in Fig. 4.25. When the RC-IGBT acts as an IGBT, it is turned off with a standard gate turn-off resistance $R_{G,OFF}$, triggered by the signal pulse s. When the device is in diode mode, it is turned off with a reduced gate turn-off resistance $R_{G,OFF,D}$ ($R_{G,OFF,D} \ll R_{G,OFF}$), triggered by the signal pulse s_R. The signals s and s_R are generated by a digital platform, in this case an FPGA.

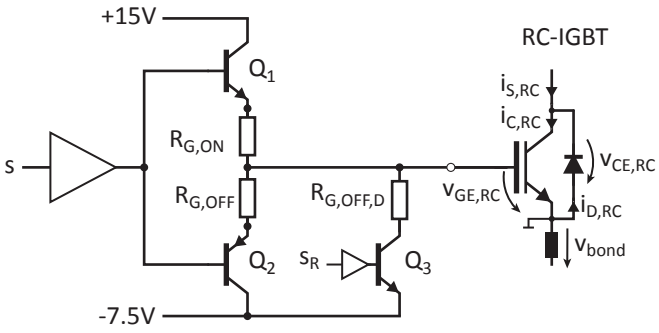


Figure 4.25: GDU output stage scheme with two gate turn-off resistances.

4.5.3 Trigger pulse generation for 2L-VSC phase leg with RC-IGBTs and sinusoidal output current *(Pulse generation)*

This section presents an algorithm to generate the trigger pulses for the RC-IGBTs including the timing for the application of the PT pulse.

Figure 4.26 shows a block diagram of the algorithm controlling a 2L-VSC phase leg. The signals s_{o1} and s_{o2} are the conventional modulation signals, generated e.g. by a PWM or a space vector modulation scheme. The signals s_{d1} and s_{d2} correspond to the modulation signals including the dead time t_{dead}.

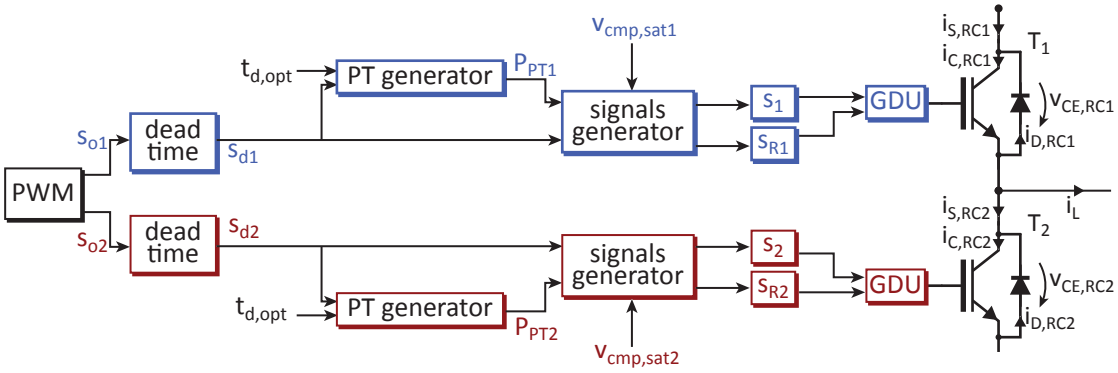


Figure 4.26: Block diagram of the algorithm to generate the trigger pulses for a 2L-VSC phase leg with RC-IGBTs.

The *PT generator* block generates the PT pulses P_{PT1} and P_{PT2} after every high to low transition of s_{d1} and s_{d2}. The *signals generator* block selects the application of the PT-pulse or the conventional modulation signal (e.g. PWM). After a low to high transition of the P_{PT1} and P_{PT2}, the state of the RC-IGBTs T_1 and T_2 (diode or IGBT mode) is acquired by the signals $v_{cmp,sat1}$ and $v_{cmp,sat2}$ respectively. If the RC-IGBT acts as a diode, its respective trigger signal s_1 or s_2 only includes the PT pulse, and the device is turned off with a reduced gate turn-off resistance $R_{G,OFF,D}$, triggered by its respective signal s_{R1} or s_{R2}. However, if the RC-IGBT acts as an IGBT, its respective trigger signal s_1 or s_2 includes the conventional modulation signals, and the device is turned off with a standard gate turn-off resistance $R_{G,OFF}$. Example waveforms can be appreciated in Fig. 4.27. The start of the PT pulse (t_{start}) is determined by

$$t_{start} = t_1 - t_0 = t_{dead} - t_{PT} + t_d, \tag{4.1}$$

where t_{dead} is the duration of the dead-time ($t_2 - t_0$), t_{PT} is the length of the PT pulse ($t_3 - t_1$) and t_d is the delay time of the PT pulse ($t_3 - t_2$).

In the example presented in Fig. 4.27 the dead time is $t_{dead} = 2\,\mu s$, the length of the PT pulse is $t_{PT} = 1.5\,\mu s$ and the delay time is $t_d = 0.5\,\mu s$. Therefore, the PT pulses P_{PT1} and P_{PT2} are generated $1\,\mu s$ ($2 - 1.5 + 0.5$) after the high to low transition of s_{d1} and s_{d2} respectively. The direction of RC-IGBT T_2 collector current $i_{S,RC2}$ is measured during the low to high transition of the PT signal P_{PT2} (instant t_1) as an input for the algorithm to determine whether the RC-IGBT T_2 acts as a diode or as an IGBT. In the case shown in the Fig. 4.27, the output load current i_L is positive, which means that RC-IGBT T_1 acts as an IGBT ($v_{cmp,sat1} = 1$) and that RC-IGBT T_2 acts as a diode ($v_{cmp,sat2} = 0$). The trigger pulses s_1 and s_2 are sent to the GDU, where s_2 only includes the PT pulse signal. After a high to low transition of the applied PT pulse, the reduced gate turn-off resistance $R_{G,OFF,D}$ is triggered by the signal s_{2R}.

It should be noted that this scheme has some complications when the load current is small or during zero-crossing. Under some circumstances, a short circuit can occur when the PT pulse is applied. An example of this situation is presented in Fig. 4.28. During the phase $t_0 - t_3$ the RC-IGBT T_2 is in the conducting state and acts as a diode. After the falling edge of the signal s_{d2} (instant t_1), the PT pulse is generated and the measurement of the signal $v_{cmp,sat2}$ is triggered at t_2. Then, the PT pulse is applied during the time interval $t_2 - t_5$.

During the time interval $t_3 - t_4$ the load current changes direction. After the current polarity change, T_2 acts as an IGBT. At t_4 the RC-IGBT T_1 is turned on. During the interval $t_4 - t_5$ both semiconductors are in the conduction state and in IGBT mode, which causes a short circuit for a short period of time. After the turn-off of the PT pulse at t_5, the short circuit stops and the RC-IGBT T_1 is in the conduction state. It should be noted that the turn-off transient of a short circuit current with the low gate resistance $R_{G,OFF,D}$ could lead to large over-voltages which could destroy the RC-IGBT.

In order to avoid this possible short circuit, the PT pulse is not applied for small current levels, as shown in Fig. 4.29. If the load current $|i_L| \leq |I_{L,lim}|$ (gray area), the PT pulses are disabled and standard modulation pulses are applied ($t_2 - t_3$).

A current limit $I_{L,lim}$ is defined by the following equation:

$$I_{L,lim} \geq \frac{di}{dt} \cdot t_{PT}. \tag{4.2}$$

A typical di_C/dt of the load current for IGBTs with a rating of 200 A for motor drive applications is around 0.23 A/µs. Therefore the minimum value of the current limit $I_{L,lim}$ where the PT pulse should be disabled is:

$$I_{L,lim} \geq 0.23\,\frac{A}{\mu s} \cdot 1.5\,\mu s \geq 0.345\,A. \tag{4.3}$$

The current limit $I_{L,lim}$ can be adjusted by modifying the value of the reference voltage ($V_{ref,sat}$) in the current direction detection scheme (Fig. 4.23). Even if a safety margin is used for the choice of $I_{L,lim}$, the current band in which conventional gate signals are applied is small in comparison to the peak converter current, so that the negative influence on converter losses is low.

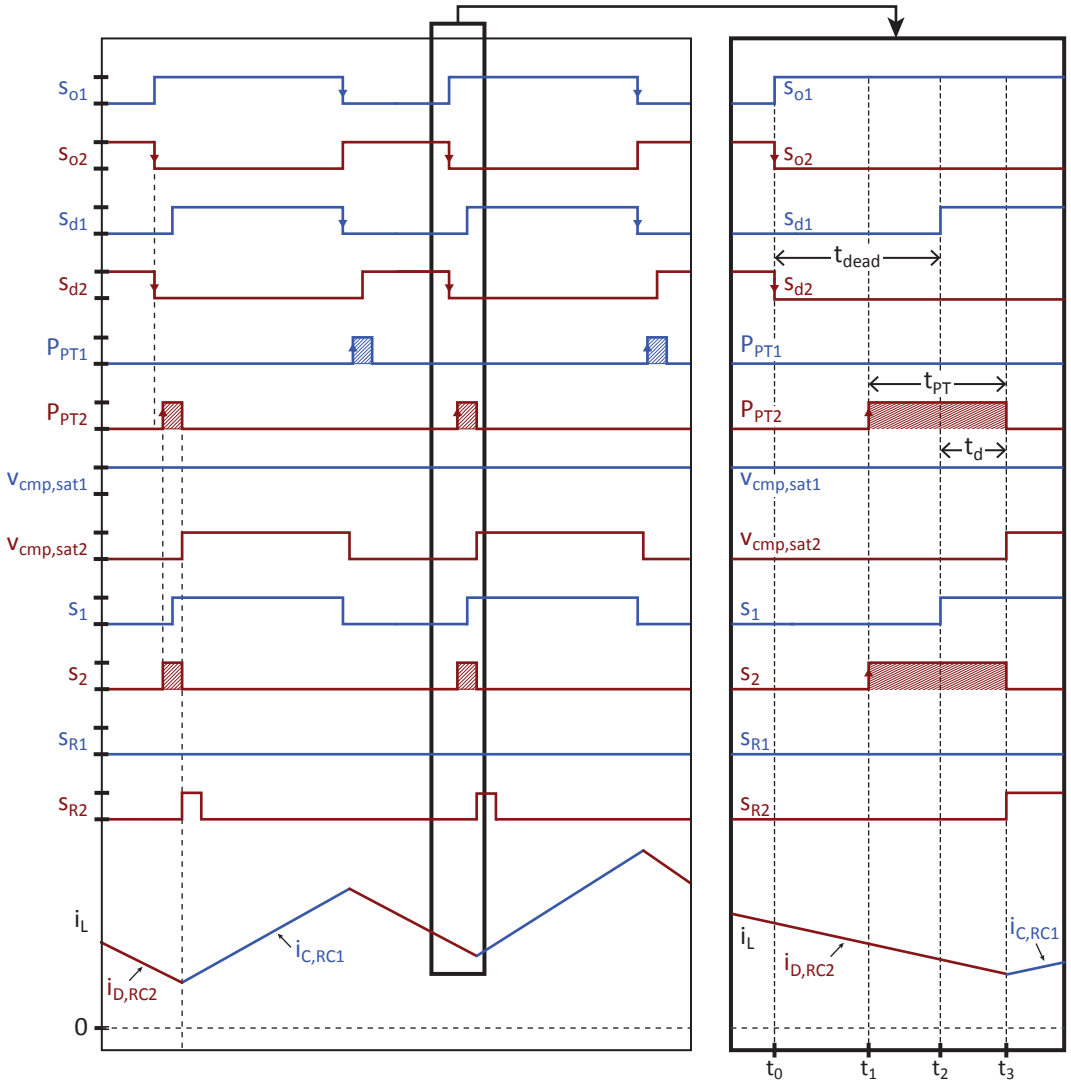


Figure 4.27: Ideal waveforms of the scheme to generate the optimized trigger pulse of a 2L-VSC converter with RC-IGBT.

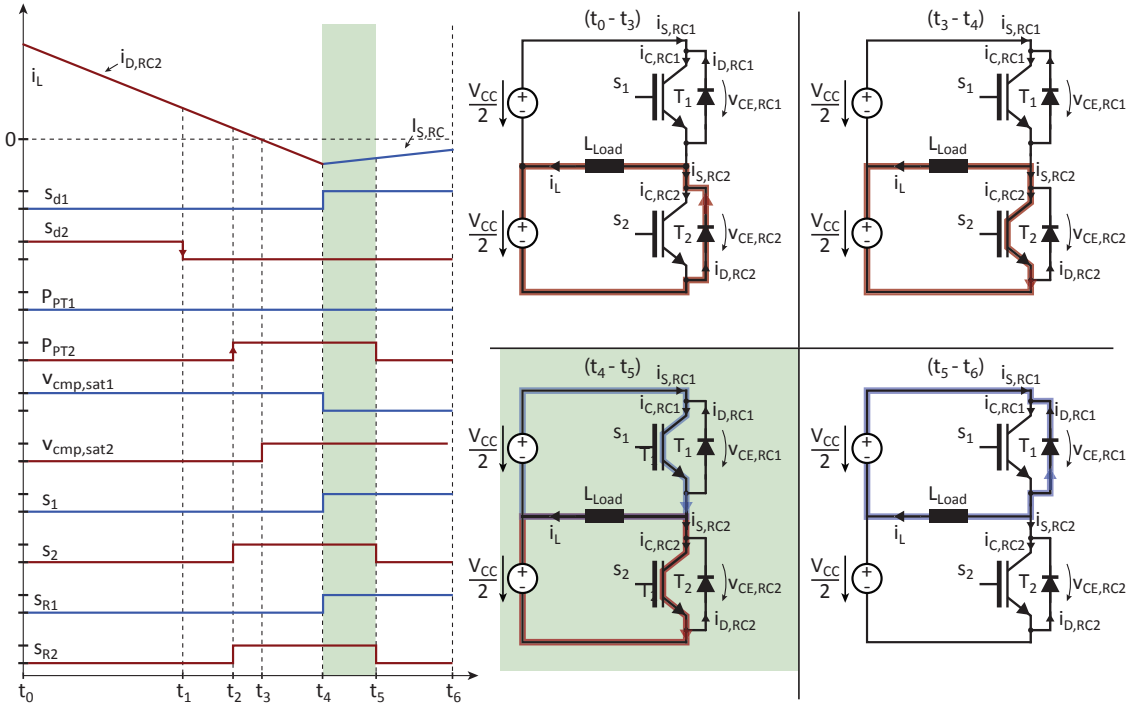


Figure 4.28: Example of a short circuit situation in an RC-IGBT with PT pulse.

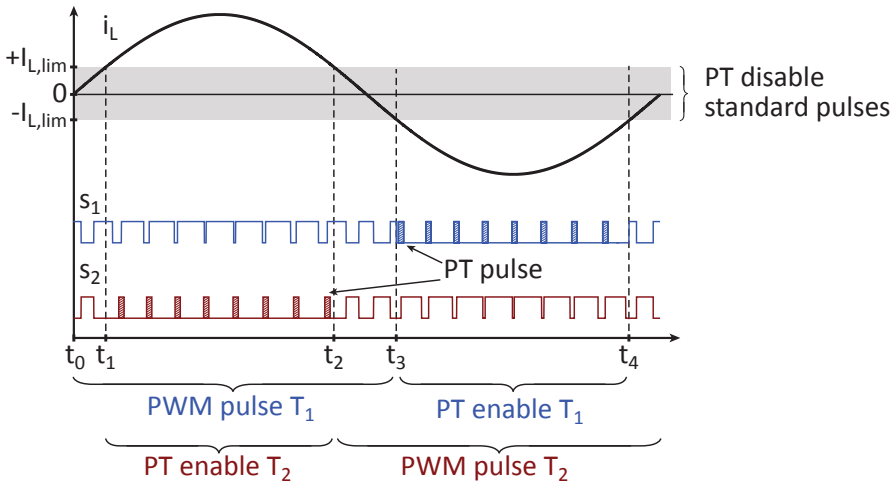


Figure 4.29: Ideal waveforms of the control strategy for a 2L-VSC phase leg with RC-IGBTs and current limitation for the application of the PT pulse.

4.5.4 Experimental results

The pulse generation was experimentally tested in one phase of a 2L-VSC converter, as shown in Fig. 4.30. The high-side semiconductor device (T_1) is an RC-IGBT and the low-side switch (T_2) is a standard IGBT with an inverse diode. Throughout the test, the RC-IGBT is operated in diode mode. Table 4.6 summarizes the test conditions.

Table 4.6: Test conditions for the investigation of the optimized pulse generation

Variable	Value	Description
V_{CC}	75 V	DC-link voltage
L	152 µH	Load inductance
di_C/dt	0.23 A/µs	Maximal current change rate
T_j	25°C	Ambient temperature
t_{PT}	1.5 µs	Pre-trigger pulse length
T_1	—	Reverse conducting IGBT (RC-IGBT) 200 A / 1200 V
T_2	FF650R17IE4	650 A / 1700 V IGBT from Infineon

Three different situations were studied: a positive load current, a negative load current and a current zero-crossing situation.

The experimental results are presented in Fig. 4.31, which depicts the collector current through the IGBT ($i_{C,T}$), the current through the diode of the RC-IGBT ($i_{D,RC}$), the $V_{CE,sat}$ measurement of the RC-IGBT $V_{CEm,sat}$ (defined in Fig. 4.23), the indicator of the state of the RC-IGBT signal in the on-state mode ($v_{cmp,sat}$), the gate-emitter voltage of the IGBT (v_{GE}) and the gate-emitter voltage of the RC-IGBT ($v_{GE,RC}$).

The RC-IGBT acts as a diode during $t < 1100$ µs, and therefore the PWM signal is disabled and the PT pulse is enabled, but during $t > 1100$ µs the RC-IGBT acts as an IGBT. Consequently the PWM signal is enabled and the PT pulse is disabled for the RC-IGBT.

Results for a positive load current i_L are presented in Fig. 4.32. In this case, the RC-IGBT acts as a diode, which means the PT pulse is applied. This is evident in the gate-emitter voltage $v_{GE,RC}$ of the RC-IGBT, where the PT pulse is applied approximately between 725 and 726.5 µs. The discharge of the RC-IGBT input capacitance lasts approximately 300 ns, due to the reduced gate turn-off resistance $R_{G,OFF,D}$. The measurement of $V_{CE,sat}$ and consequently the signal $v_{cmp,sat}$

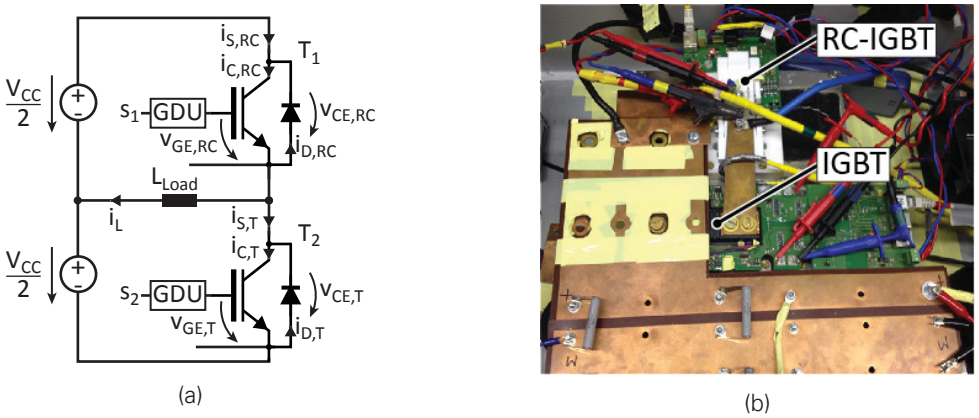


Figure 4.30: Equivalent circuit and photo of 2L-VSC phase leg for the verification of the proposed pulse generation scheme.

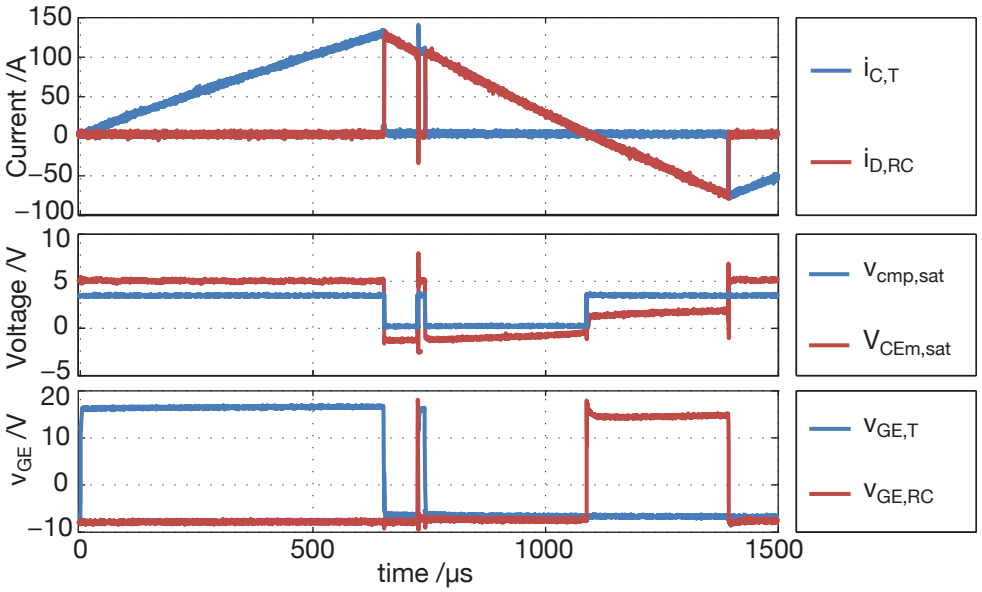


Figure 4.31: Experimental results of the proposed pulse generation for the RC-IGBT (V_{CC} = 75 V, T_j = 25°C).

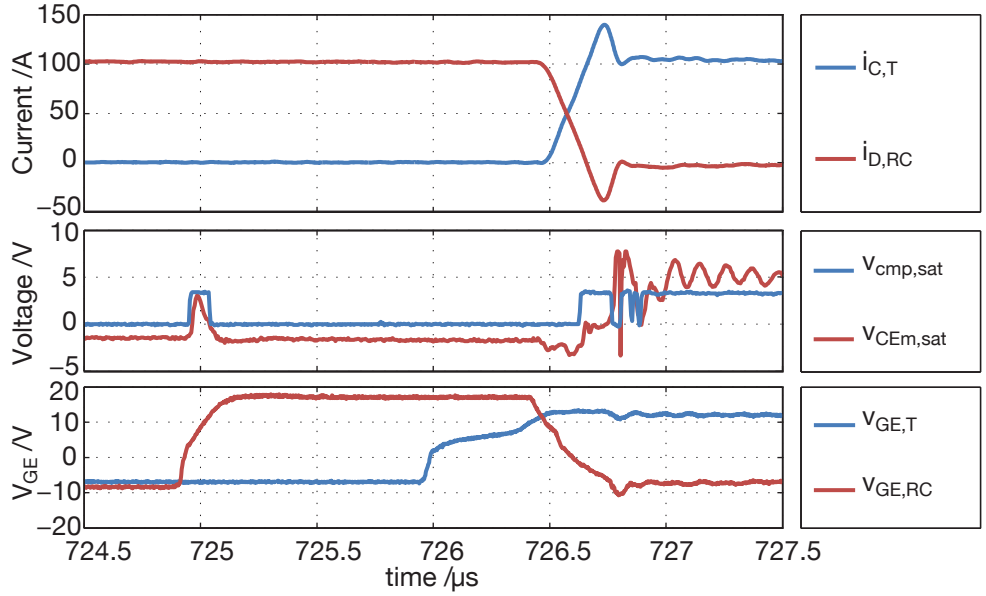


Figure 4.32: Experimental results, detailed view on a positive current $i_{D,RC}$ (V_{CC} = 75 V, T_j = 25°C).

presents a disturbance influenced by the gate-emitter voltage of the RC-IGBT and by the occurring $di_{D,RC}/dt$.

When the load current i_L is negative, see Fig. 4.33, the RC-IGBT operates in IGBT mode. Therefore, the conventional PWM signal is applied. This can be seen by way of the gate-emitter voltage of the RC-IGBT $v_{GE,RC}$, where the PWM signal terminates before the turn-on of IGBT T_2, due to the dead time. The input capacitance of the RC-IGBT is discharged in around 900 ns through the standard gate turn-off resistance $R_{G,OFF}$. The oscillation of $V_{CE,sat}$ and the voltage spike of $v_{cmp,sat}$ are caused by EMI disturbances (in particular the $di_{D,RC}/dt$).

A zero-crossing situation of the load current i_L is presented in Fig. 4.34. The collector-emitter voltage v_{CE} changes from negative to positive which leads to a change of polarity of $v_{cmp,sat}$.

When the collector current $i_{D,RC}$ is lower than 1 A, $v_{cmp,sat}$ changes from 0 to 1 enabling the PWM signals and disabling the PT pulse. In this case, the current limit $I_{L,lim}$ is 1 A, allowing safe operation of the 2L-VSC with RC-IGBTs. The oscillations of $v_{cmp,sat}$ can be reduced by increasing the hysteresis of the comparator.

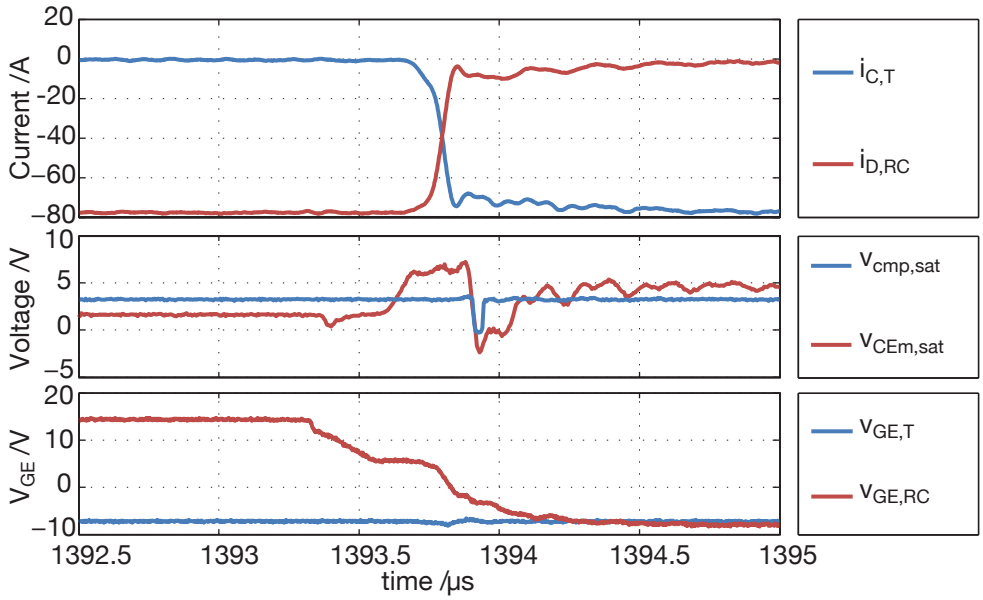


Figure 4.33: Experimental results, detailed view with a negative current $i_{D,RC}$ (V_{CC} = 75 V, T_j = 25°C).

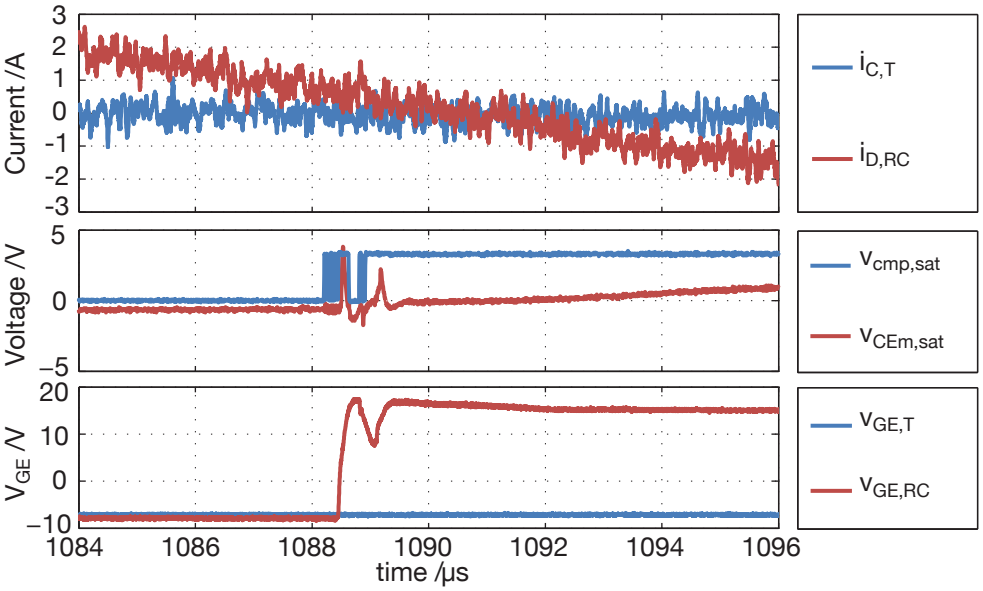


Figure 4.34: Experimental results, detailed view of zero-crossing of the current $i_{D,RC}$ (V_{CC} = 75 V, T_j = 25°C).

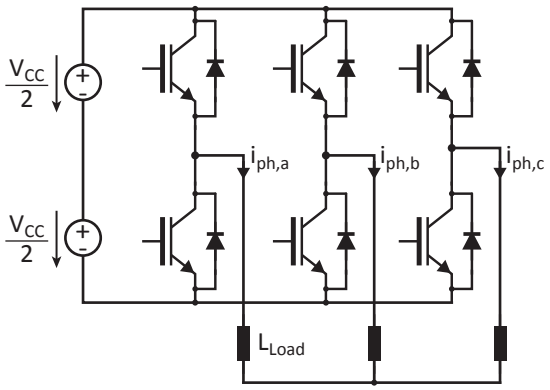


Figure 4.35: 2L-VSC converter topology used in the simulation.

4.5.5 Saving potential of switching losses

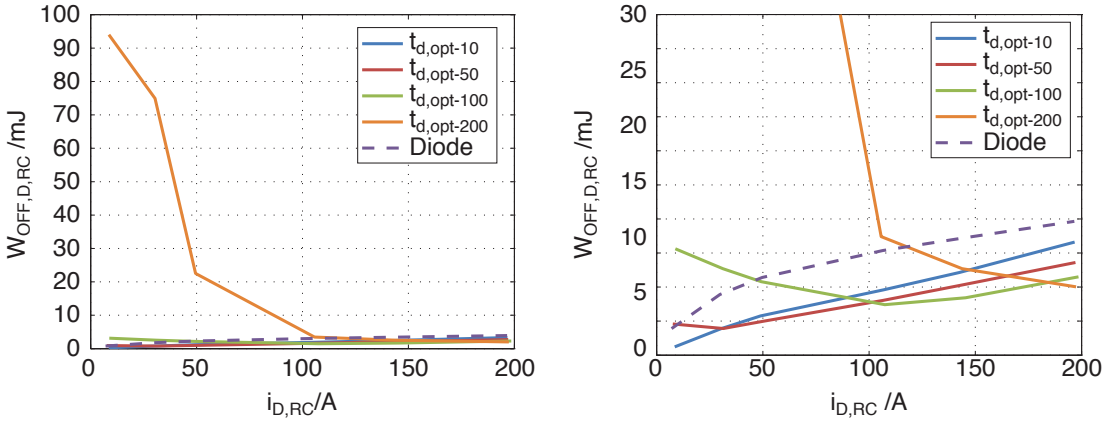
A simple realization of the PT pulse can be achieved if the optimal delay time $t_{d,opt}$ obtained automatically remains constant during the entire load current range of operation for a given converter. The results presented in Section 4.3.2 showed that an adaptation of $t_{d,opt}$ to the current value can be avoided for DC-Link voltage $V_{CC} \geq 500\,V$. Despite of the slight dependency of $t_{d,opt}$ on the collector current, there is a specific value which minimizes the total switching losses of a 2L-VSC (Fig. 4.35). Therefore, the converter with IGBT and RC-IGBTs operating in diode mode has been simulated with MATLAB, Simulink and PLECS to calculate the converter losses for different values of $t_{d,opt}$. The device switching losses for the simulation have been experimentally obtained and adapted to the simulation conditions.

Fig. 4.36 shows device switching losses of the turn-off transient of the RC-IGBT operating in diode mode ($W_{OFF,D,RC}$). During the experimental investigation, four $t_{d,opt}$ values were determined at four different current levels: 10 A ($t_{d,opt\text{-}10}$), 50 A ($t_{d,opt\text{-}50}$), 100 A ($t_{d,opt\text{-}100}$) and 200 A ($t_{d,opt\text{-}200}$). These value of $t_{d,opt}$ were applied to the entire current load range $10\,A < i_L < 200\,A$ and the switching losses were compared to the switching losses of a standard diode (Diode). The experimental results show high switching losses when the calculated $t_{d,opt\text{-}200}$ is used with a collector current of 10 A. The corresponding turn-off losses $W_{OFF,D,RC}$ are approximately 95 times higher than the separate diode switching losses, whereas, with a $t_{d,opt\text{-}200}$ for a collector current of 200 A, the switching losses are reduced by 50% compared to the standard diode.

Fig. 4.37a shows the IGBT turn-on losses of the IGBT ($W_{ON,T}$). Applying the value $t_{d,opt\text{-}200}$ to a collector current of 10 A causes an increase of the switching losses by a factor of 5 compared to the losses when a separate diode is used, whereas when the collector current is 200 A, the losses are reduced by approximately 13%.

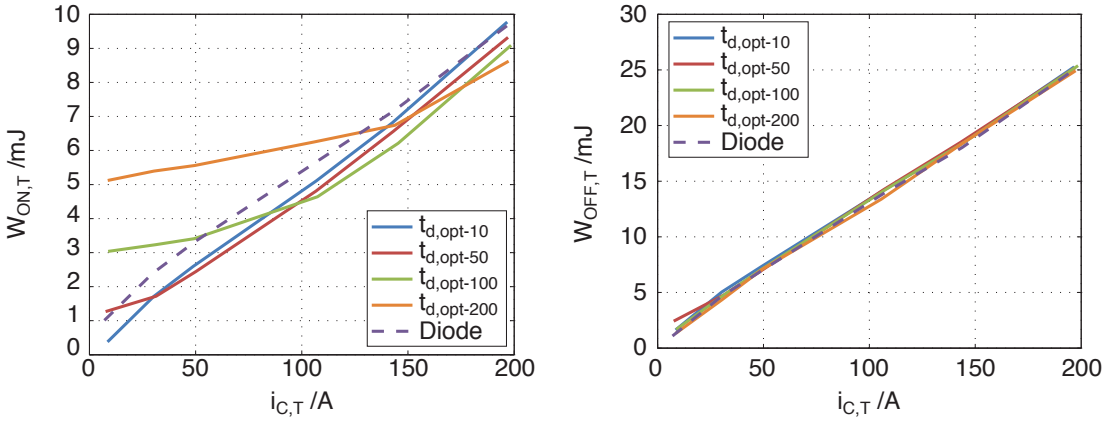
4.5.5.1 Simulation of the 2L-VSC with sinusoidal load current

A 2L-VSC with a sinusoidal load current was simulated to estimate the potential reduction of losses when RC-IGBTs with suitable trigger pulses are used instead of separate diodes. Six different simulation configurations (SimC) have been simulated and analysed. In the simulation, the RC-IGBT is in diode mode. The simulation conditions and the simulation configurations are presented in Table 4.7.



(a) Large scale (b) Zoom-in

Figure 4.36: Device turn-off losses $W_{\mathrm{OFF,D,RC}}$ for different $t_{\mathrm{d,opt}}$ (V_{CC} = 500 V, T_{j} = 25°C).



(a) Turn-on transient (b) Turn-off transient

Figure 4.37: IGBT switching losses for different $t_{\mathrm{d,opt}}$ (V_{CC} = 500 V, T_{j} = 25°C).

Table 4.7: Conditions of the simulation of the 2L-VSC with sinusoidal load current

Variable	Description
V_{CC}	750 V
i_{ph}	100 A rms
T_{j}	25 °C
Power Factor $\cos\varphi$	1 and −1
Switching frequency f_{sw}	4 kHz
PWM modulation index m_{a}	0.88
Simulation configuration 1 (SimC1)	IGBTs with separate diodes
Simulation configuration 2 (SimC2)	IGBTs with RC-IGBTs, $t_{\mathrm{d}} = t_{\mathrm{d,opt\text{-}10}}$
Simulation configuration 3 (SimC3)	IGBTs with RC-IGBTs, $t_{\mathrm{d}} = t_{\mathrm{d,opt\text{-}50}}$
Simulation configuration 4 (SimC4)	IGBTs with RC-IGBTs, $t_{\mathrm{d}} = t_{\mathrm{d,opt\text{-}100}}$
Simulation configuration 5 (SimC5)	IGBTs with RC-IGBTs, $t_{\mathrm{d}} = t_{\mathrm{d,opt\text{-}200}}$
Simulation configuration 6 (SimC6)	IGBTs with RC-IGBTs without PT pulse

The simulation has been carried out according to the 2L-VSC converter and the IGBT models described in [53, 54]. The results of the simulation with a power factor $\cos\varphi$ = 1 are shown in Fig. 4.38 and Table 4.8. The figure and table show the conduction power losses $P_{\mathrm{CON,T}}$ for the

IGBT and $P_{CON,D,RC}$ for the RC-IGBT, the turn-off power losses $P_{OFF,T}$ for the IGBT and $P_{OFF,D,RC}$ for the RC-IGBT and the turn-on power losses $P_{ON,T}$ for the IGBT. Additionally, the table shows the total power losses, defined by:

$$P_{Total} = P_{CON,T} + P_{OFF,T} + P_{ON,T} + P_{CON,D,RC} + P_{OFF,D,RC}. \tag{4.4}$$

Moreover, the results are compared to the total power losses when a separate diode is used instead of an RC-IGBT.

The lowest total losses were obtained with simulation configuration 3 (SimC3), where 11.7% of the total losses are IGBT turn-on power losses ($P_{ON,T}$) and 4.1% are diode turn-off power losses of an RC-IGBT ($P_{OFF,D,RC}$). Moreover, the total losses of the converter were reduced by 3.2% compared to the losses of a converter with separate diodes. If the RC-IGBT is used with conventional PWM gate signal pulses (SimC6), the total power losses are increased by 23.7% compared to the power losses of a converter with separate diodes.

Table 4.8: Power loss distribution for $\cos\varphi = 1$

Test	IGBT			Diode/RC-IGBT		P_{Total} /W	Comparison in %
	$P_{CON,T}$ /W	$P_{OFF,T}$ /W	$P_{ON,T}$ /W	$P_{CON,D,RC}$ /W	$P_{OFF,D,RC}$ /W		
SimC1	45.3 [40.2 %]	35.1 [31.2 %]	14.8 [13.1 %]	9.4 [8.3 %]	8.10 [7.2 %]	112.7 [100 %]	100 %
SimC2	45.3 [41.2 %]	36.2 [32.9 %]	13.1 [11.9 %]	10.4 [9.4 %]	5 [4.5 %]	109.9 [100 %]	97.5 %
SimC3	45.3 [41.5 %]	36.3 [33.3 %]	12.7 [11.7 %]	10.4 [9.5 %]	4.4 [4.1 %]	109.2 [100 %]	96.8 %
SimC4	45.3 [40.9 %]	35.8 [32.3 %]	13.7 [12.3 %]	10.4 [9.3 %]	5.8 [5.2 %]	111 [100 %]	98.4 %
SimC5	45.3 [26 %]	35 [20.1 %]	18.3 [10.5 %]	10.4 [5.9 %]	65.3 [37.5 %]	174.3 [100 %]	154.6 %
SimC6	45.3 [32.5 %]	36.2 [25.9 %]	24.3 [17.4 %]	15.4 [11 %]	18.3 [13.1 %]	139.5 [100 %]	123.7 %

When the 2L-VSC is used in generation mode ($\cos\varphi = -1$), the total power losses using RC-IGBTs and SimC3 are 0.7% higher than the losses using separate diodes (Fig. 4.39 and Table 4.9), due to the higher conduction losses of the RC-IGBT compared to a standard diode. When the RC-IGBT is used with conventional PWM gate signal pulses, the power losses are 46.1% higher than the power losses of a converter with diodes.

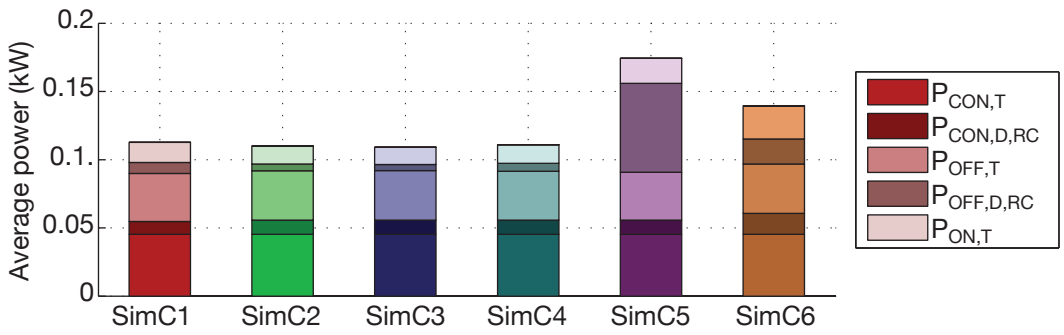


Figure 4.38: Simulated power losses of a 2L-VSC with sinusoidal load current (V_{CC} = 750V, $i_{ph,RMS}$ = 100 A, f_{sw} = 4 kHz, $\cos\varphi$ = 1, m_a = 0.88).

For a power factor of $\cos\varphi = 1$, the configuration with RC-IGBTs showed slightly lower power losses than the configuration with IGBTs and separate diodes, with a total power loss reduction of approximately 3.2%. However, for a power factor of $\cos\varphi = -1$ the configuration with RC-IGBTs and the configuration with separate diodes demonstrated comparable power loss.

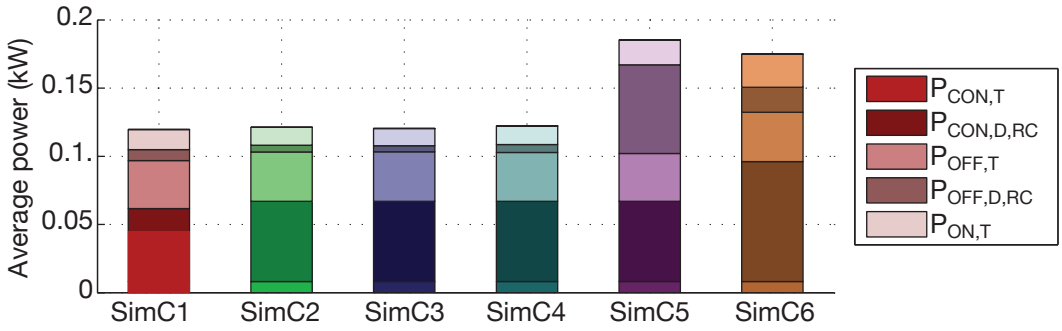


Figure 4.39: Simulated power losses of a 2L-VSC with sinusoidal load current (V_{CC} = 750V, $i_{ph,RMS}$ = 100 A, f_{sw} = 4 kHz,$\cos\varphi$ = -1, m_a = 0.88).

Table 4.9: Power loss distribution for $\cos\varphi = -1$

Test	IGBT			Diode/RC-IGBT		P_{Total} /W	Comparison in %
	$P_{CON,T}$ /W	$P_{OFF,T}$ /W	$P_{ON,T}$ /W	$P_{CON,D,RC}$ /W	$P_{OFF,D,RC}$ /W		
SimC1	8.1 [6.7 %]	35.1 [29.4 %]	14.8 [12.3 %]	53.6 [44.8 %]	8.1 [6.8 %]	119.6 [100 %]	100 %
SimC2	8.1 [6.6 %]	36.2 [29.8 %]	13.1 [10.8 %]	58.9 [48.6 %]	5 [4.1 %]	121.2 [100 %]	101.3 %
SimC3	8.1 [6.7 %]	36.3 [.2 %]	12.7 [10.6 %]	58.9 [48.9 %]	4.4 [3.7 %]	120.4 [100 %]	100.7 %
SimC4	8.1 [6.6 %]	35.9 [29.3 %]	13.6 [11.2 %]	58.9 [48.2 %]	5.8 [4.7 %]	122.2 [100 %]	102.1 %
SimC5	8.1 [4.3 %]	35 [18.9 %]	18.2 [9.8 %]	58.9 [31.8 %]	65.1 [35.1 %]	185.3 [100 %]	154.9 %
SimC6	8.1 [4.6 %]	36.2 [20.7 %]	24.3 [13.9 %]	88 [50.3 %]	18.3 [10.5 %]	174.9 [100 %]	146.1 %

4.6 IMPLEMENTATION CONSIDERATIONS

For the above-mentioned investigations, a GDU was designed to accomplish the basic technological requirements of RC-IGBTs. The GDU, shown in Fig. 4.40, consists of the following main blocks.

- **Communication stage:** connects the GDU with the FPGA through cat 5e cables and differential line receiver/transmitter
- **Isolation stage:** isolates the control signals from the high power signals with a maximum working insulation voltage of 1414 V and 150 Mbps of signal rate
- **Power supply:** generates supply voltages of +15 V and −7.5 V for the output stage.
- **Power stage:** recharges the RC-IGBT input capacitances using a push-pull amplifier
- **Measurement stage:** measures v_{bond} voltage of the semiconductor in order to estimate the current through the device, and measures the $V_{CE,sat}$ voltage in order to determine the current direction through the semiconductor

A block diagram of the GDU is presented in Fig 4.41. The GDU is controlled by an external control platform, based on a Spartan-3 FPGA from Xilinx. The FPGA and the GDU are connected through twisted pair cables (cat 5e). The number of necessary connections is the main disadvantage of this implementation. There are 5 signals from the FPGA to the GDU and 3 signals from the GDU to the FPGA. In total, this implementation needs 8 communication signals. The limited number of ports on industrial control platforms as well as costs and reliability considerations are the main reason, therefore, that the realized GDU concept would require changes for adaptation into a real industrial application.

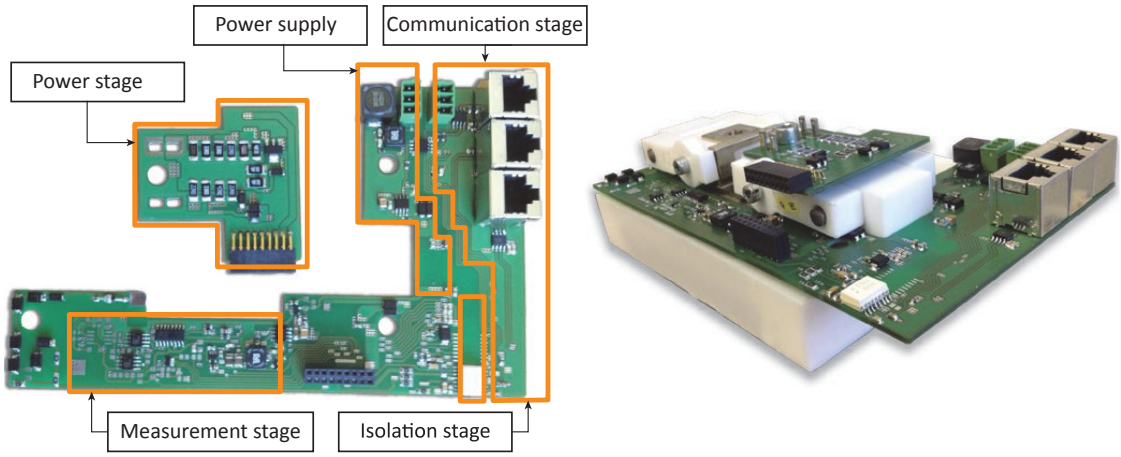


Figure 4.40: PCB of the GDU prototype to control the RC-IGBT.

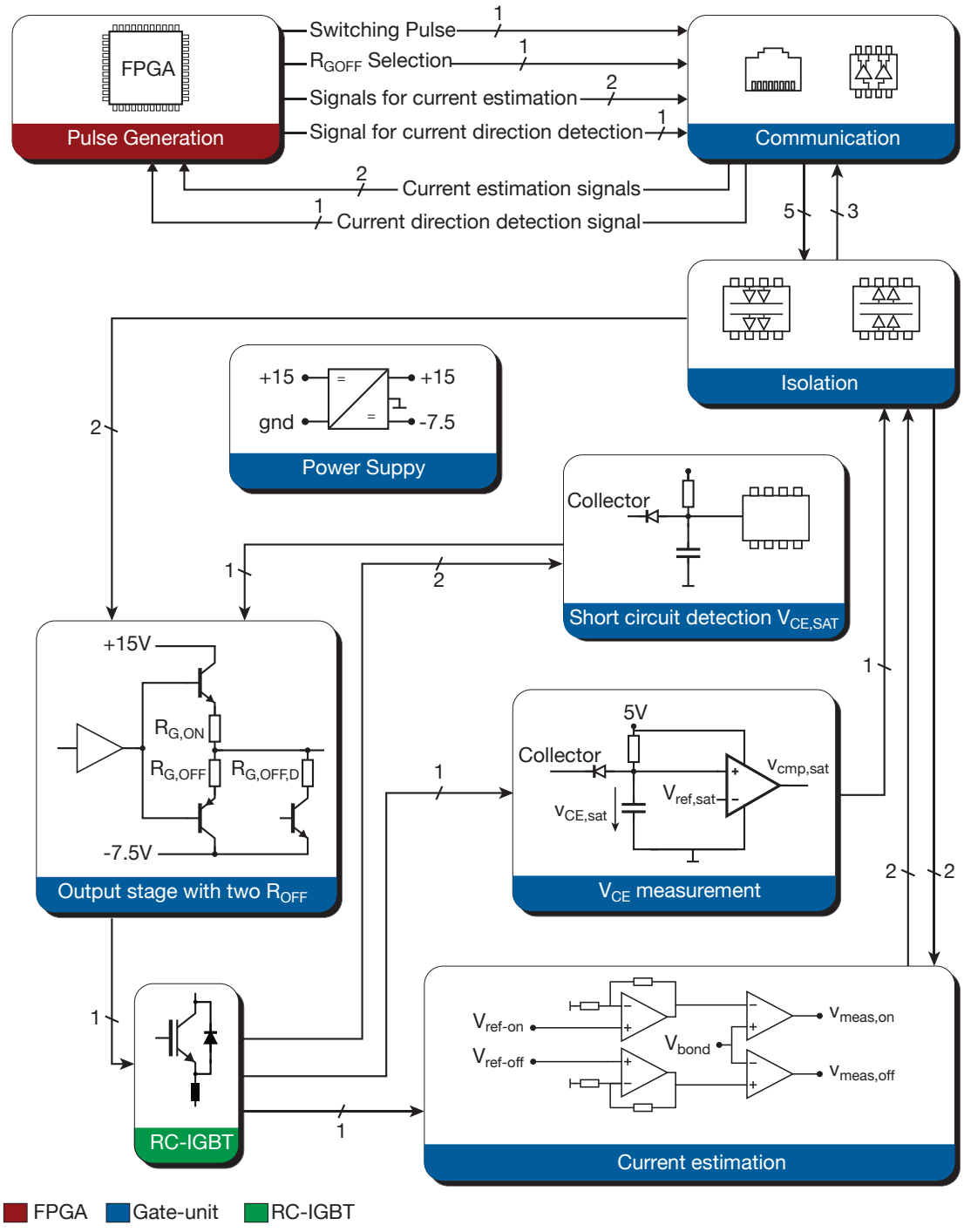


Figure 4.41: Functional block diagram of the GDU concept for the RC-IGBT.

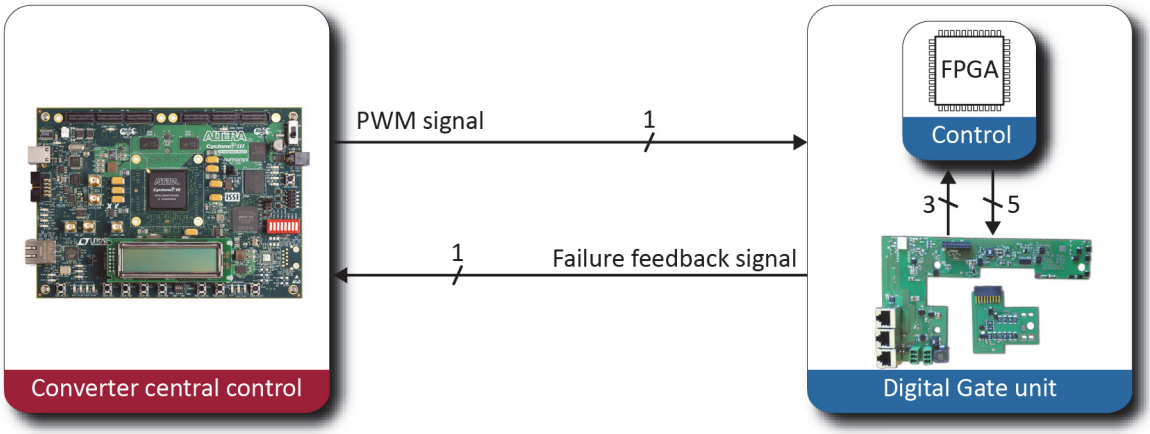


Figure 4.42: Block diagram of a proposed digital GDU for the RC-IGBT.

One possible realization option for an industrial implementation could be a digital GDU, which includes a micro-controller or an FPGA. In that case the central control unit could send normal modulation pulses to the GDU, and the GDU generates and controls the application of the PT pulse independently. A diagram of the proposed solution is presented in Fig. 4.42. This proposal would need two communication signals, one from the central control to the GDU and one vice versa, using a suitable communications protocol.

4.7 SUMMARY

This chapter presented the investigation of a feasible scheme to operate RC-IGBTs with reduced losses compared to a conventional PWM scheme. In the first section, the structure and function of the RC-IGBT were described. The losses of the RC-IGBT operating in diode mode can be reduced by applying a desaturation pulse before and during the diode turn-off transient [12], and during the conduction state by setting the gate-emitter voltage of the RC-IGBT to a value below 0 V ($v_{GE,RC} < 0$ V).

The second and third sections showed the experimental investigation of the influence of the PT pulse on the switching losses. An optimal delay time $t_{d,opt}$ of the PT pulse can reduce the switching losses e.g. by 35% in the IGBT and by 60% in the RC-IGBT in diode mode, compared to the switching losses when a RC-IGBT without a PT pulse is used. Compared with a standard diode, the RC-IGBT with a PT pulse demonstrated e.g. 20% lower turn-off losses, and also reduced the turn-on losses of an IGBT e.g. by 25%.

According to the investigation, the pulse length of the PT pulse t_{PT} can remain constant and should be longer than 1.5 µs in order to minimize the switching losses. Moreover, the RC-IGBT should be controlled with two different gate turn-off resistances. If the RC-IGBT acts as a diode, the gate turn-off resistance value $R_{G,OFF,D}$ of the RC-IGBT must be as low as possible.

The optimal delay time $t_{d,opt}$ of the PT pulse only slightly depends on the collector current and T_j when the DC-Link voltage V_{CC} is higher than 500 V. Therefore, $t_{d,opt}$ can be found at one collector current level and be applied for the entire current operating range of the device. However, a deviation of ±40 ns from $t_{d,opt}$ causes an increases of the switching losses and could even cause a short circuit, so appropriate protection measures must be taken.

A scheme to find the value $t_{d,opt}$ automatically was presented in the fourth section, where the current through the RC-IGBT is estimated with the sensed voltage across the emitter stray inductance. The fifth section presented a scheme to generate the GDU signals suitable for a 2L-VSC

converter with RC-IGBTs. Thus, the conduction losses can be reduced by 60% compared to the losses of the RC-IGBT with conventional signals. This scheme also includes a strategy to avoid possible short circuits.

In addition, a 2L-VSC configuration with RC-IGBTs instead of one with a separate diode was simulated to investigate the power losses. The simulation results showed a power loss reduction of about 3.2% of the total power losses for a power factor $\cos\varphi = 1$. For a power factor $\cos\varphi = -1$ the RC-IGBT and the switch configuration with a separate diode had similar power losses.

The RC-IGBT can be an alternative to a conventional IGBT–diode configuration. However, this semiconductor device requires extra effort to generate suitable trigger signals. Nevertheless, the concepts presented in this chapter provide ideas and options for possible industrial implementations, in particular for 2L-VSC converters.

5 SELECTED GATE DRIVE UNIT INNOVATIONS

This chapter presents new concepts for various GDU functions. The following topics are addressed:

- Static balancing of IGBTs connected in parallel,
- fast short circuit protection,
- switching loss reduction , and
- operation of IGBTs with a higher gate-emitter voltage.

The GDU function concepts have been experimentally tested in a buck converter with primePACK^{TM} IGBT modules. For each GDU concept, the principle, design, implementation (hardware and software) and the experimental results are presented and analysed in the following sections.

5.1 STATIC BALANCING OF IGBTS CONNECTED IN PARALLEL

The increasing demand for large converter power ratings and the physically limited maximum current of semiconductor devices have made a parallel connection of these an attractive approach for high power applications. The parallel connection of IGBTs is already a widely used approach in high power converters. However, the current through the IGBTs may not be symmetrically distributed between the parallel-connected switches, as shown in Fig. 5.1. The imbalance may be caused by differences of device parameters such as $V_{CE,sat}$, $V_{GE,th}$, internal gate resistances, and/or GDU differences (e.g. time delays in the gate signals, differences of $R_{G,ON}$, etc) or an asymmetrical power part (e.g. regarding stray inductance). Current imbalance occurs during the on-state (static operation) and/or during switching transients (dynamic operation). An imbalance of the collector currents limits device utilization and converter power.

The dynamic imbalance can be addressed using a GDU with di_C/dt control, as published in [55], or with a delay time compensation method [40, 56, 57]. In the latter, the dynamic imbalance is compensated by delaying the gate signals of the parallel connected IGBTs. The optimal delay time can be found by measuring the collector current with a Rogowski coil [56]. A simpler method

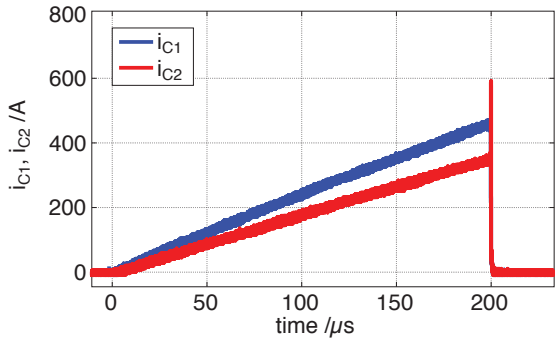


Figure 5.1: Current imbalance in two parallel connected IGBTs in the on-state.

based on a delay time compensation scheme has been proposed in [40, 57]. In this scheme, the power-emitter to auxiliary-emitter voltage is used as an indirect measurement of the collector current changes. An algorithm determines the corresponding delay time differences between the collector currents i_C of parallel connected IGBTs. This new scheme provides an inexpensive and reliable delay time compensation for achieving symmetrical collector currents at the turn-on and turn-off transients of parallel connected IGBTs.

In order to achieve a current balance in the on-state of IGBTs connected in parallel, various approaches have been proposed. Most of them are based on device de-rating and/or selection. However, a de-rating of the semiconductors devices [58, 59] reduces die utilization and, consequently, increases costs. Selecting semiconductor devices [58, 59] according to certain device parameters (e.g. gate-emitter threshold voltage, switching times, on-state voltage, etc.) causes additional costs as well as presenting challenges for service and maintenance.

Collector currents in the on-state of parallel connected IGBTs can be balanced by means of an active adjustment of the gate-emitter voltage, and a measurement of the collector current [60–62]. Additional current sensors are needed to implement this scheme, which reduces the versatility of this approach.

One measure to achieve balanced currents is a symmetrical power part design (e.g. regarding stray inductances) [63–65]. But this approach generates higher development and manufacturing costs. Besides, it adds limitations to the mechanical layout and design of the converter.

This section considers the current balancing of parallel connected IGBTs in the on-state. The proposed concept is simple and the additional expense is low.

5.1.1 Principle of the method

The new method for the static balancing of the collector currents is based on the dependency of the conductivity of the IGBT on the gate-emitter voltage v_{GE}. The output characteristics of two IGBTs connected in parallel at two different gate-emitter voltages v_{GE} is shown in Fig. 5.2. IGBTs connected in parallel share the same saturation collector emitter voltage $V_{CE,sat}$. The IGBTs conduct different collector currents at different gate-emitter voltages, v_{GE1} and v_{GE2}.

Figure 5.3 shows the output characteristics of the (1400 A / 1200 V) IGBT FF1400R12IP4 from Infineon as an example. The IGBT conducts 1100 A at a gate-emitter voltage v_{GE} of 13 V and $V_{CE,sat}$ of 2 V. However, using a gate-emitter voltage v_{GE} of 15 V, the collector current is approximately 1250 A.

The collector currents through the IGBTs connected in parallel are balanced by means of the active control of the gate-emitter voltages v_{GE}. A balance controller calculates a correction factor

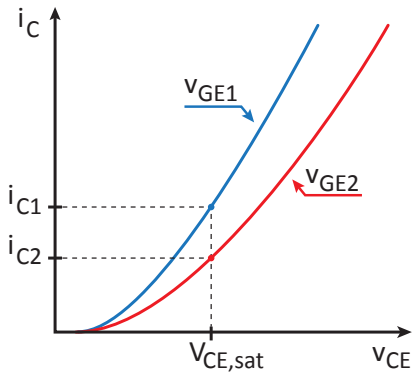


Figure 5.2: Principle output characteristics of an IGBT with different gate-emitter voltages, where $v_{GE1} > v_{GE2}$.

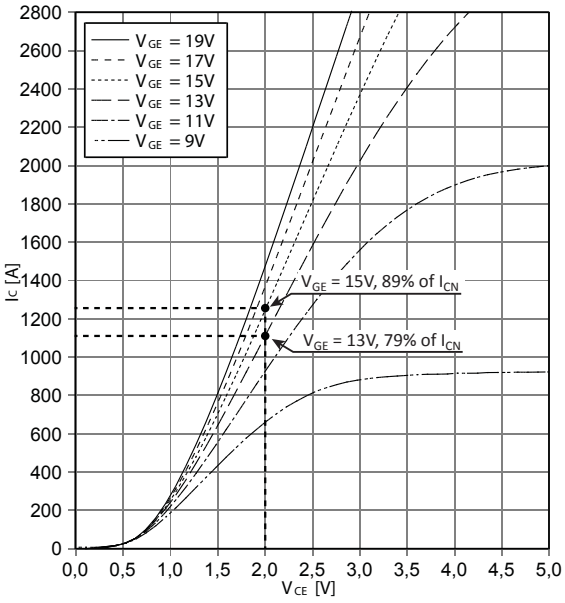


Figure 5.3: Output characteristics $i_C = f(v_{CE})$, (1400 A / 1200 V) IGBT FF1400R12IP4, T_j = 150°C.

for each current, which corresponds with either a reduction or an increase of each gate-emitter voltage. For example, if two IGBTs are connected in parallel and the first IGBT carries 25% more current than the second IGBT, the currents could be balanced in the following manner: The gate-emitter voltage of the first IGBT is reduced, which increases the on-state voltage of the first IGBT for a given current. That means the resulting on-state resistance is increased. As a consequence, the current through the second IGBT is increased, the current through the first IGBT is reduced and the collector emitter voltage is increased. Alternatively, the gate-emitter voltage of the second IGBT could be increased. This would decrease the on-state voltage of the second IGBT for a given current and decrease the resulting on-state resistance. As a consequence, the current carried by the first IGBT would decrease. However, to ensure safe performance, the gate-emitter voltage must not exceed the maximum allowable gate-emitter voltage, or other limitations imposed upon this voltage, for example by short circuit operation, EMI issues, etc.

In order to determine the amount of stationary imbalance of the currents through the switches, the currents can be estimated using the method proposed in Section 3.1. As an alternative, the current can be measured using current sensors such as Rogowski coils, Hall-effect or other measurement devices. However, it is not necessary to know precise current values, but only the ratio(s) of the currents with respect to each other, which can be determined quite simply by using the method described in Sec. 3.1.

5.1.2 Control of the gate-emitter voltage v_{GE}

A block diagram of the GDU concept is shown in Fig. 5.4, where the IGBT is turned on and off with MOSFETs in a half-bridge configuration. Moreover, the turn-on gate-emitter voltage V_{GEon} can be modified by the gate unit power supply which includes a controllable DC-DC converter.

5.1.2.1 Gate unit power supply

As presented in Fig. 5.4, an IGBT driver is used as a push-pull output stage for a pulse transformer. The control signal c_S is a pulse-width modulated signal with a carrier frequency of 100 kHz. The

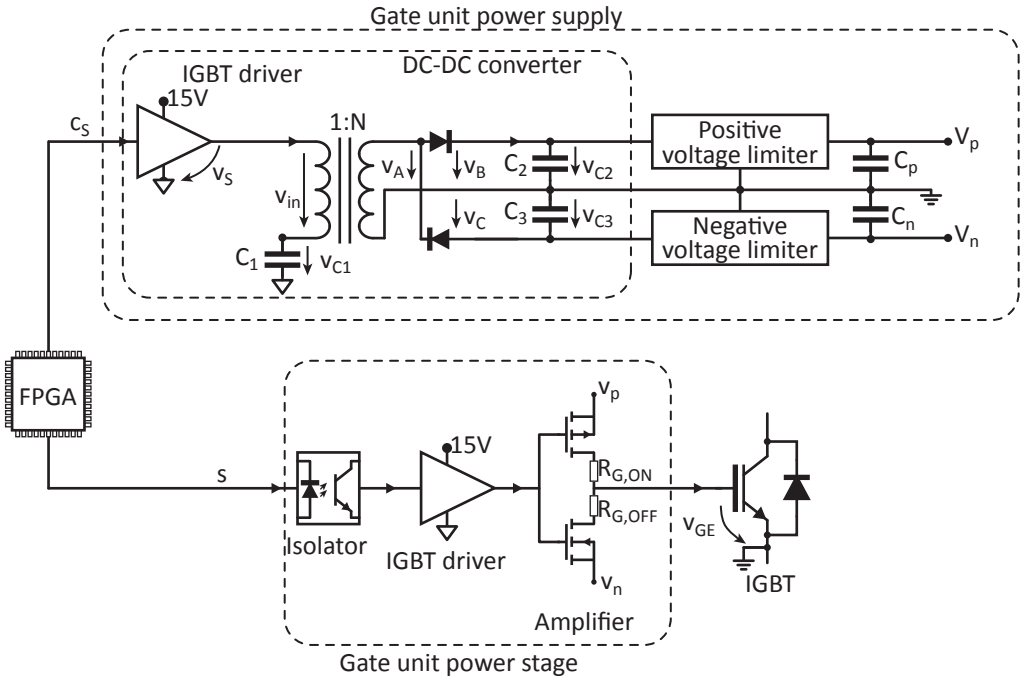


Figure 5.4: Block diagram of the GDU concept with v_{GE} modification.

voltage v_S alternates between 0 V and 15 V with the same frequency and duty cycle as c_S. The primary winding is connected in series with the capacitor C_1, which generates a duty cycle dependent bias voltage $v_{C1} = D_C \cdot 15\,\text{V}$, where D_C is the duty cycle of c_S. The voltage $v_{in} = V_S - v_{C1}$ induces a voltage v_A on the secondary winding of the transformer, which has a turns ratio of 1:2.4. The diodes rectify this voltage into two output voltages v_{C2} and v_{C3}. These voltages are limited by positive and negative voltage limiters. By altering the duty cycle of the PWM signal c_S and, thus, the voltage v_{C1}, it is possible to alter the positive supply voltage V_p and the negative supply voltage V_p.

As an example, the operation of the controlled DC-DC power supply is shown in Figure 5.5 at two different duty cycles, 50% and 80%. Figure 5.5a shows the power supply operation with a duty cycle of c_S equal to 50%. The output voltage of the IGBT driver v_S alternates between 0 and 15 V. The voltage of the capacitor C_1 v_{C1} corresponds to the mean value of v_S, with an average of 7.5 V. The voltage v_{in} alternates between −7.5 V and +7.5 V, and the voltage v_A, which alternates between −18 V and +18 V, is rectified by the diodes. Thereby, v_{C2} and v_{C3} amount to +18 V and −18 V, respectively. After the positive and negative voltage limiters, the voltage V_p and V_n are V_p = +18 V and V_n = −8 V.

Figure 5.5b presents the power supply operation for a duty cycle D_C = 80%. Thus v_{C1} is 12 V in average. The voltage v_{in} alternates between −12 V and +3 V. The voltage at the secondary winding of the pulse transformer v_A alternates between −28.8 V and +7.2 V. The voltage at the capacitor C_2 is v_{C2} = +7.2 V and at the capacitor C_3 is v_{C3} = −28.8 V. After their corresponding voltage regulators, the positive output voltage V_p = +7.2 V and the negative output voltage V_n = −8 V.

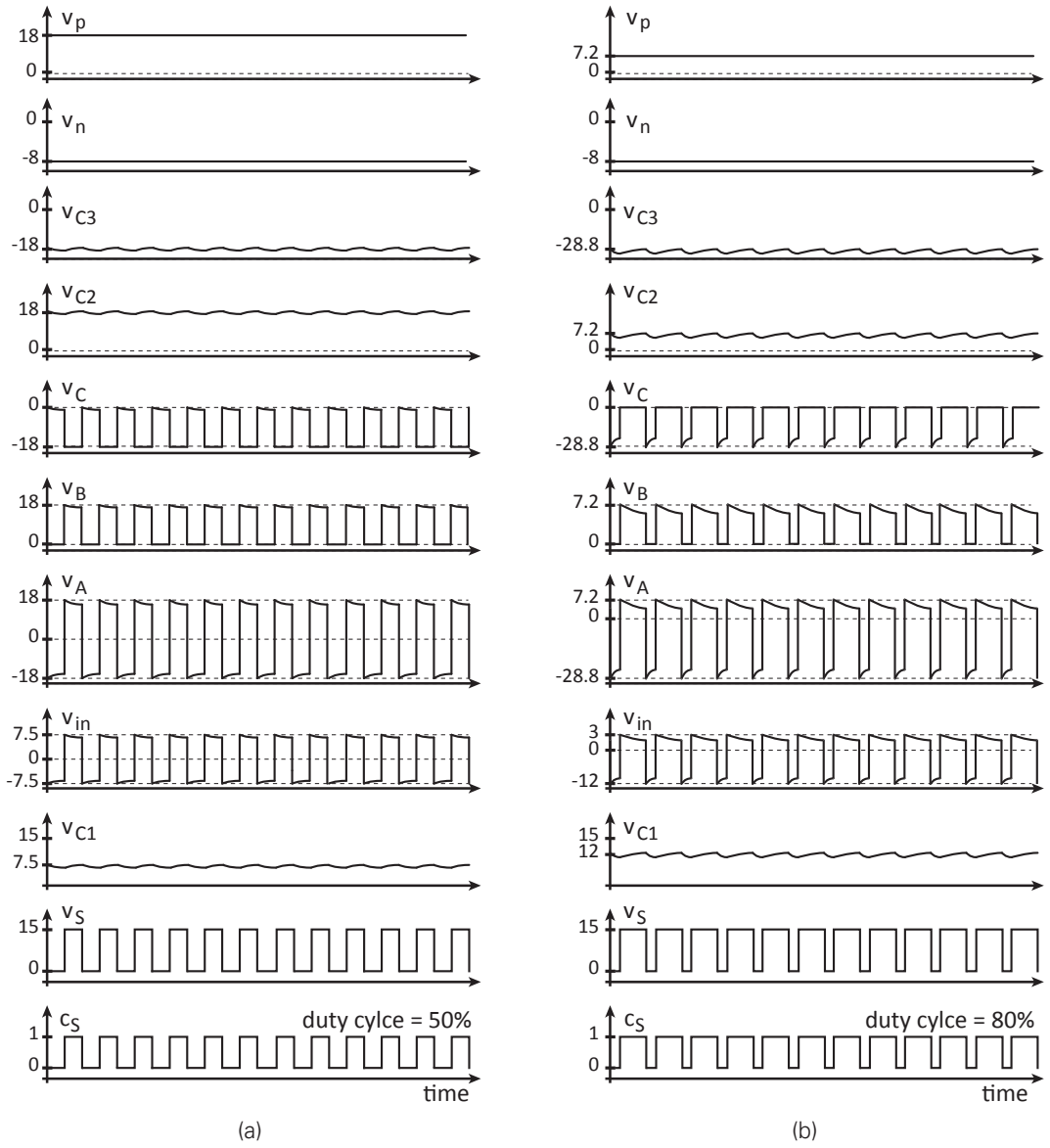


Figure 5.5: Example of the DC-DC power supply operation. (a) D_C= 50%, and (b) D_C= 80%.

5.1.2.2 Concept for a faster adjustment of the gate-emitter voltage

Turning on the IGBTs with different gate-emitter voltages causes a coupling between the stationary and the dynamic current balancing [40]. In order to decouple them, both IGBTs are turned on with V_{GEon} = 15 V and after the turn-on transient, the gate-emitter voltage v_{GE} is modified if a balancing of the collector currents is required.

Balancing the stationary currents by means of the duty ratio of the proposed DC-DC converter has several advantages, such as simplicity, stability and robustness. However, the method has slow dynamics because of the relatively high output capacitances of the DC-DC converters. This can be improved by using smaller output capacitances C_2, C_3, C_p and C_n. However, smaller capacitances also increase the voltage ripple of the output voltages, thus, deteriorating the stability of the system.

An alternative or additional way to achieve a higher dynamic of v_{GE} changes, is the modulation of the gate-emitter voltage of the IGBT at a high frequency through the digital command signal s (Fig. 5.4). The internal gate-emitter capacitance C_{GE}, the collector-gate capacitance C_{CG},

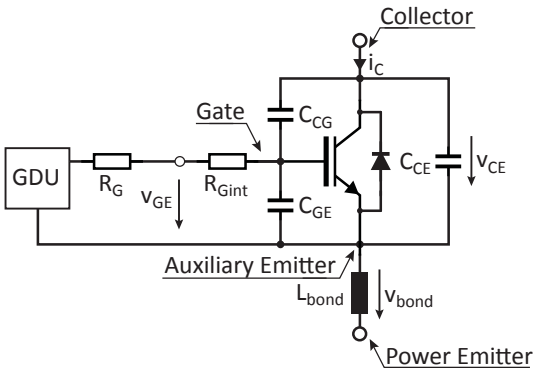


Figure 5.6: Representation of an IGBT with internal capacitances and internal and external gate resistance.

the internal and external gate resistors $R_{G,int}$ and R_G form an *RC* low pass filter, as presented in Fig. 5.6. The cut-off frequency of this filter ($\sim$2 MHz), for the considered (650 A, / 1700 V) IGBT FF650R17IE4, depends on the capacitances C_{GE} and C_{CG} and the total gate resistance ($R_{G,int} + R_G$). When the switching frequency of the trigger signal s is substantially higher than the cut-off frequency of the low-pass filter, the gate-emitter voltage v_{GE} is filtered and the high frequency is sufficiently attenuated at the gate terminal of the device.

Fig. 5.7 shows ideal waveforms of the supply unit and the power stage with a high frequency modulation of the trigger signal s. The IGBT is turned on at the instant t_1. Thus, the gate-emitter voltage rises to the positive supply voltage V_p which is at the voltage level $+V$. The trigger signal s is held high until the turn-on transient of the IGBT has ended.

From instant t_2, s is pulse-width modulated at a constant duty cycle and the gate-emitter voltage v_{GE} decreases rapidly. v_{GE} shows a fast dynamic response e.g. less than 3 µs for a step from 15 to 11 V for the considered (650 A, / 1700 V) IGBT FF650R17IE4. However, the positive supply voltage V_p shows a significant voltage drop which also affects the stability of the generated gate-emitter voltage v_{GE}.

A fast dynamic response and a stable gate-emitter voltage can be achieved by combining the proposed gate unit power supply concept with a high frequency PWM modulation of the IGBT trigger signal. Fig. 5.8 shows an example of the waveforms for this method. At first, the supply voltage $V_p = +V$ is generated using a first duty cycle d_1 of the control signal c_S.

The IGBT is turned on at instant t_1 by setting the signal s to 1 and it is held in the on-state until the IGBT turn-on transient has ended. At instant t_2 (e.g. $t_2 - t_1 = 5\,\mu s$), the signal s is pulse-width modulated at high frequency, the signal c_S is set to zero, and thus, V_p drops rapidly to the second voltage level $+V'$. At instant t_3, the PWM of s is stopped and the signal s is held high. The signal c_S starts again with a new duty cycle d_2, which keeps the voltage level $+V'$. In this example, $+V'$ is the desired voltage level for balancing the collector currents.

This method achieves a fast dynamic response e.g. v_{GE} is modified from v_{GE} = 15 V to v_{GE} = 12 V in less than 5 µs for the considered (650 A, / 1700 V) IGBT FF650R17IE4, and it features excellent stability of v_{GE} after adjusting V_p to the desired voltage $+V'$.

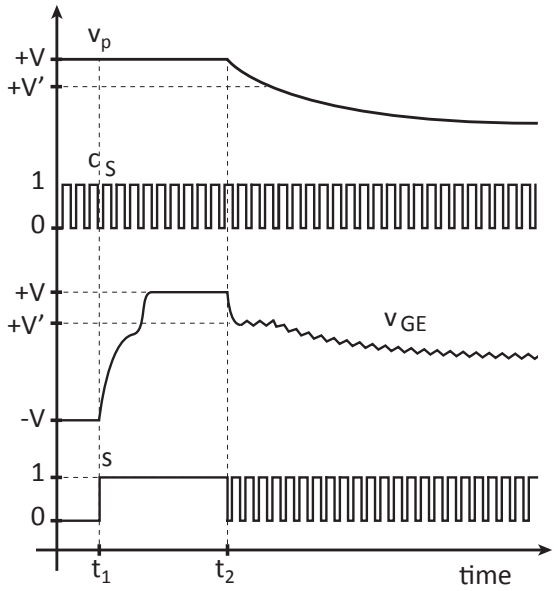


Figure 5.7: Power supply voltage V_p, gate-emitter voltage v_{GE} and FPGA pulses for the gate-emitter voltage variation method with a fast dynamic response

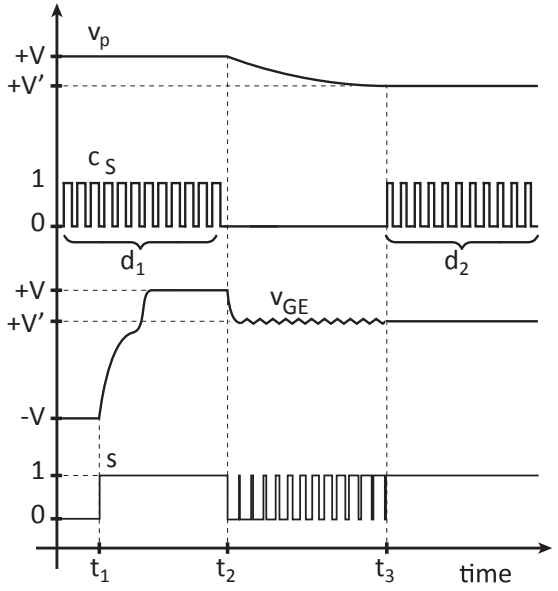


Figure 5.8: Power supply voltage V_p, gate-emitter voltage v_{GE} and FPGA pulses for the gate-emitter voltage variation method with a fast dynamic response and v_{GE} stability of the adjustment.

5.1.3 Experimental verification

5.1.3.1 Gate drive unit description

A GDU featuring a variable gate-emitter voltage and the current estimation methods presented in Section 3.1 was designed and built. The GDU is able to control a dual IGBT module with a PrimePACK housing. Fig. 5.9 shows the GDU prototype, where the different functions are highlighted. These comprise:

- A communication stage, which connects the GDU whit the FPGA through a cat 5e cable and high speed differential drivers.
- An isolation stage, which isolates the control signal of the communication stage from the signals of the power stage with a signal rate of 150 Mbps.
- A power supply, where variable voltages for the output stage are generated and voltages are controlled by a PWM signal from the FPGA.
- A power stage, where the IGBT input capacitances are recharged using a push-pull amplifier.
- A measurement stage, which uses the voltage between power and auxiliary emitter to estimate the collector current.

The interaction between the GDU stages and the FPGA is outlined in Fig. 5.10. The number of communication signals is indicated.

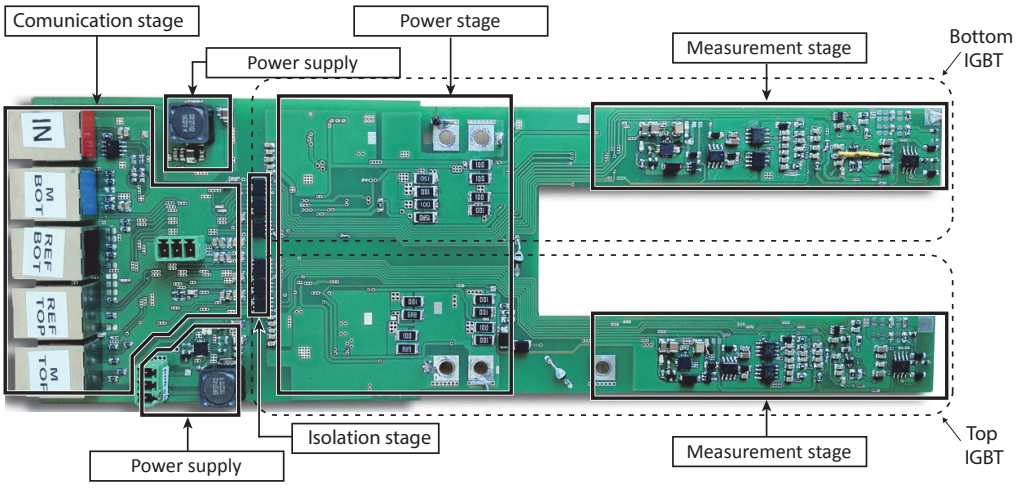


Figure 5.9: Gate unit PCB prototype for the static current balancing of IGBTs connected in parallel.

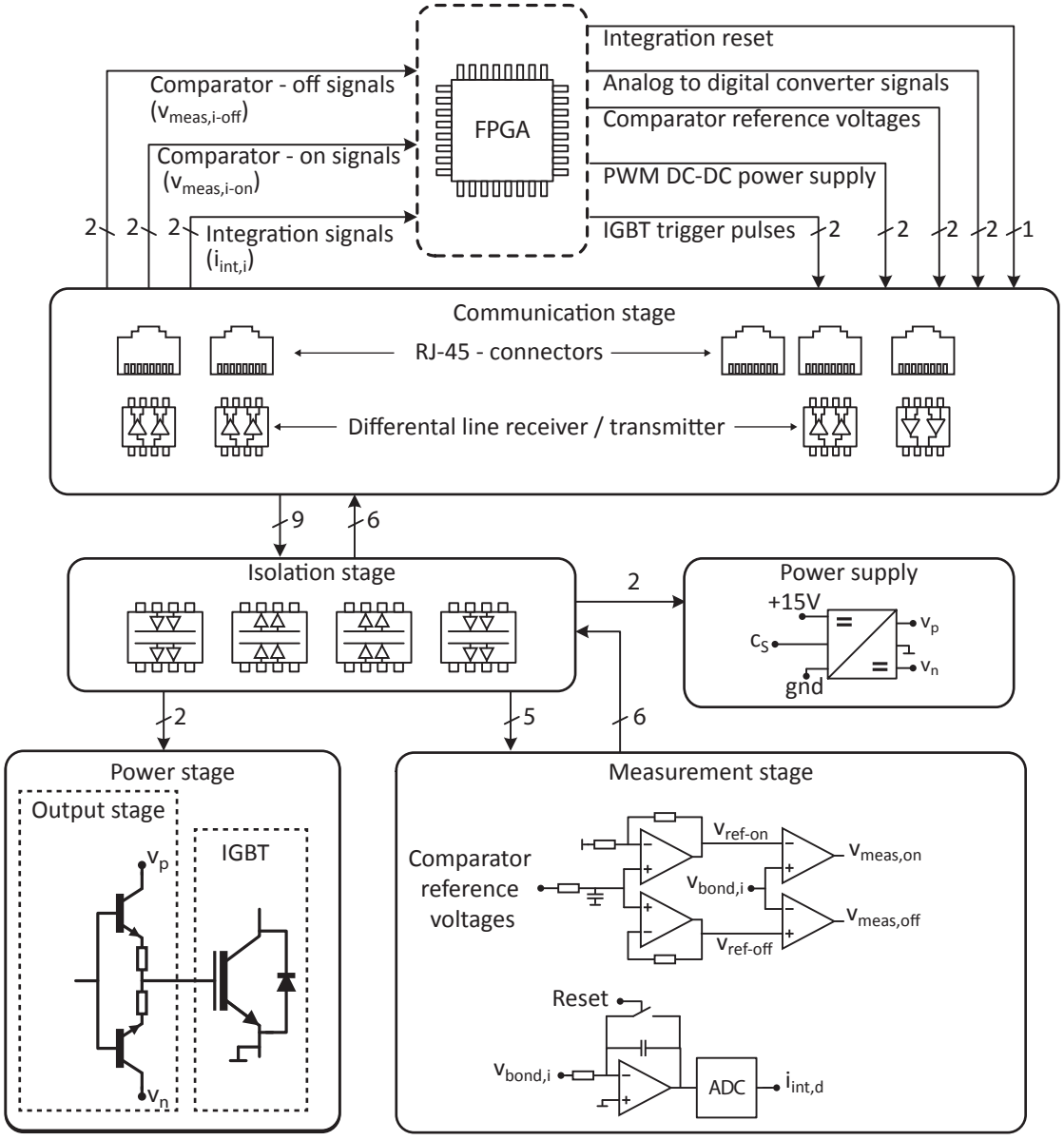
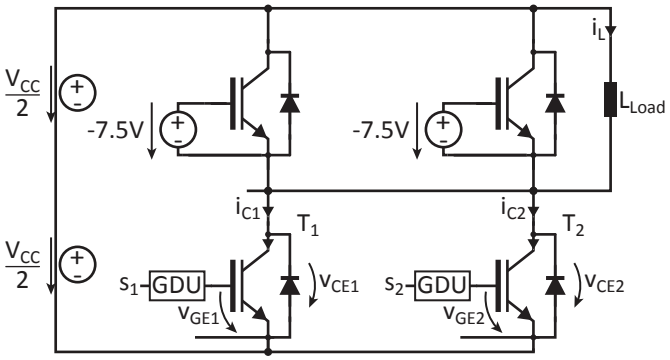
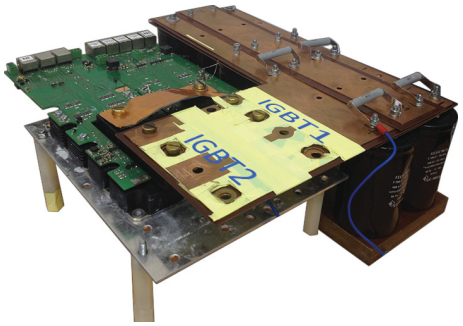


Figure 5.10: Block diagram of the GDU prototype for the static current balancing of IGBTs connected in parallel.



(a) Experimental set-up circuit (T_1 and T_2: DUT).



(b) Photograph of the set-up.

Figure 5.11: Set-up used for the verification of the scheme to balance the current of parallel connected IGBTs.

5.1.3.2 Test description

A double-pulse test was used. The gate-emitter voltage v_{GE} is actively adjusted. The topology and a picture of the test prototype are presented in Fig. 5.11. Two half bridge IGBTs, T_1 and T_2, are connected in parallel in a buck converter. They are triggered by the signals s_1 and s_2 respectively. The mechanical layout of the set-up results in an asymmetric stray inductance L_σ for the IGBTs connected in parallel. The test conditions are listed in the Table 5.1.

Table 5.1: Test conditions for the investigation of the static balancing of parallel connected IGBTs

Variable	Value
T_1, T_2	FF650R17IE4 (650 A / 1700 V)
V_{CC}	100...400 V
I_C	100...400 A
T_j	25 °C
PWM gate signal frequency	2 MHz

5.1.3.3 Experimental results

Experimental results without any current balancing method (dynamic, stationary) are shown in Fig. 5.12. Fig. 5.12a shows the collector currents of the IGBTs during their on-state. Fig. 5.12b shows the gate-emitter voltages of the IGBTs. Figures 5.12c and 5.12d show the collector currents during the turn-on and turn-off transients, respectively. Figures 5.12e and 5.12f show the gate-emitter voltages during the turn-on and turn-off transients, respectively.

The collector currents have a stationary imbalance of 100 A during the on-state at a total collector current $i_{C1} + i_{C2}$= 800 A. The imbalance is defined as:

$$\text{Imbalance} = \left| \frac{i_{C1} - i_{C2}}{0.5 \cdot (i_{C1} + i_{C2})} \right| \%. \tag{5.1}$$

The stationary imbalance reaches 25%. During the turn-on transient the dynamic imbalance reaches 150 A and during the turn-off transient 400 A. Both IGBTs were turned on with a gate-emitter voltage V_{GEon} of 15 V.

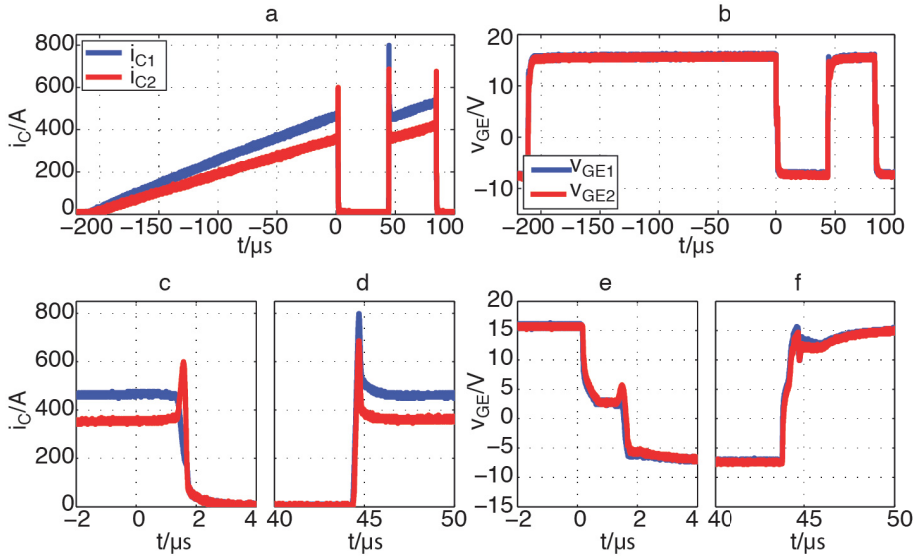


Figure 5.12: Waveform for two IGBTs connected in parallel without dynamic and static current balancing control (V_{CC} = 400 V, i_L = 800 A, T_j = 25°C). (a) Collector currents, (b) gate-emitter voltages, (c) zoom-in of the collector currents during the turn-off transient, (d) zoom-in of the collector currents during the turn-on transient, (e) zoom-in of the gate-emitter voltages during the turn-off transient and (f) zoom-in of the gate-emitter voltages during the turn-on transient.

Fig. 5.13 presents the collector currents and gate-emitter voltages when the proposed stationary current balancing scheme is used. In this case, the gate-emitter voltage is pulse-width modulated during the whole operation for simplicity, instead of modulating it during a limited period of time. The collector currents have been previously dynamically balanced using the delay time compensation method [40, 56, 57]. In this case being investigated (e.g. Fig. 5.12), the IGBT T_1 conducts a larger current than the IGBT T_2. Therefore, the gate-emitter voltage of the IGBT T_1 was reduced from 15 V to approximately 12 V, in order to reduce the current imbalance. The stationary current imbalance was reduced from 100 A to 20 A during the stationary state, which means a reduction from 25% to 5% accordingly to (5.1).

5.1.4 Closed loop control for two IGBTs connected in parallel

This section presents a closed-loop control scheme for two IGBTs connected in parallel, so that static current balancing is achieved automatically. The control algorithm was implemented in an FPGA. The balancing of the collector current of IGBTs connected in parallel depends on the accuracy of the current estimation methods.

The collector current is estimated at every turn-off transient using the method *current estimation by integration (CEI)* (Section 3.1.1). The gate-emitter voltage of the IGBT with the largest collector current is reduced automatically. A block diagram of the algorithm is presented in Fig. 5.14. The scheme operates as follows:

1. *Dynamic balancing:* The collector currents are dynamically balanced during turn-on and turn-off transients by the delay time compensation scheme proposed in references [40, 56, 57]. Therefore, the current estimation method can estimate the collector current without additional error due to dynamic imbalance [40].

2. *Estimation of the collector current:* The collector currents i_{C1} and i_{C2} are estimated during the IGBT turn-on and turn-off transients. The estimated currents are defined as $\overline{i_{C1m}}$ for the collector current of the IGBT T_1 and $\overline{i_{C2m}}$ for the collector current of the IGBT T_2.

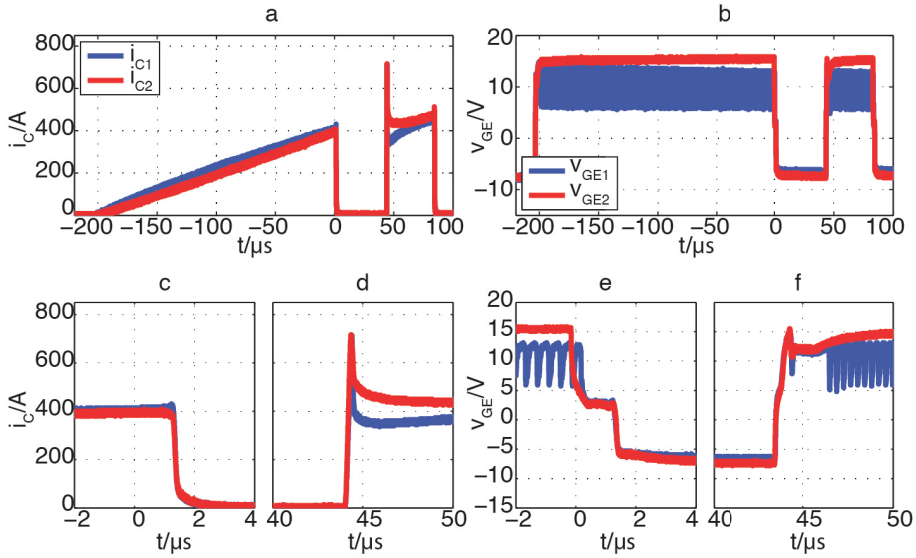


Figure 5.13: Waveforms for two IGBTs connected in parallel with dynamic and static current balancing control (V_{CC} = 400 V, i_L = 800 A, T_j = 25°C). (a) Collector currents, (b) gate-emitter voltages, (c) zoom-in of the collector currents during the turn-off transient, (d) zoom-in of the collector currents during the turn-on transient, (e) zoom-in of the gate-emitter voltages during the turn-off transient and (f) zoom-in of the gate-emitter voltages during the turn-on transient.

- If ($\overline{i_{C1m}} > \overline{i_{C2m}} + k$), the gate-emitter voltage v_{GE1} is reduced and v_{GE2} is kept at 15 V after the next turn-on transient. The block *Dynamic balancing* is repeated. The variable k is a tolerance range, which defines an imbalance tolerance band for the collector currents.
- If ($\overline{i_{C2m}} > \overline{i_{C1m}} + k$), the gate-emitter voltage v_{GE2} is reduced and v_{GE1} is kept at 15 V after the next IGBT turn-on transient. The block *Dynamic balancing* is repeated.
- If the above mentioned conditions are not fulfilled the collector current are considered as balanced, then v_{GE1} and v_{GE2} are not modified. The gate-emitter voltage combination that minimizes the collector current imbalance has been found.

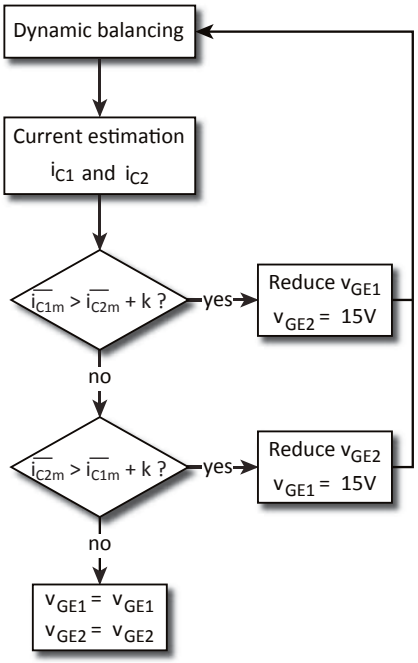


Figure 5.14: Block diagram of the closed-loop control algorithm for two IGBTs connected in parallel.

5.1.4.1 Experimental results of the closed-loop control algorithm

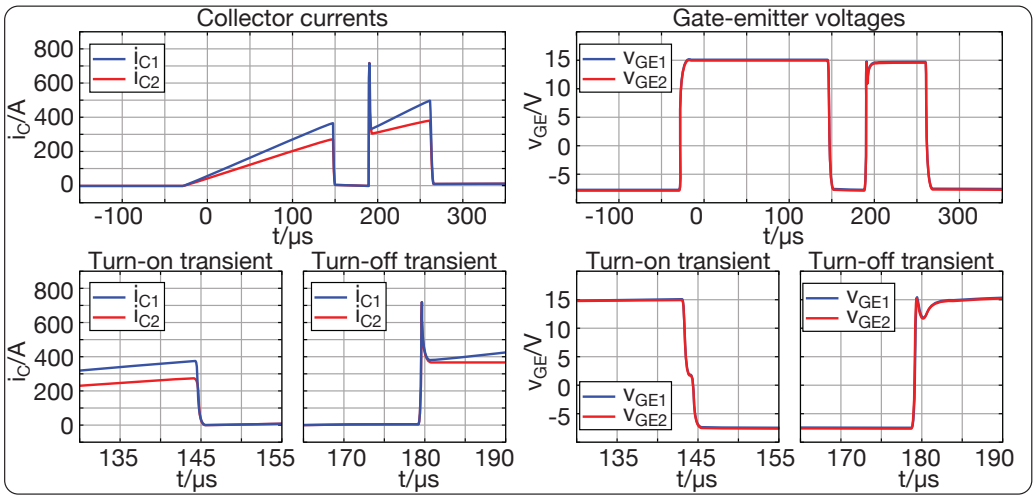
The algorithm was tested in a buck converter with two IGBT half bridge modules connected in parallel. The test conditions are listed in Table 5.1.

Table 5.2: Test conditions for the verification of the closed-loop control algorithm

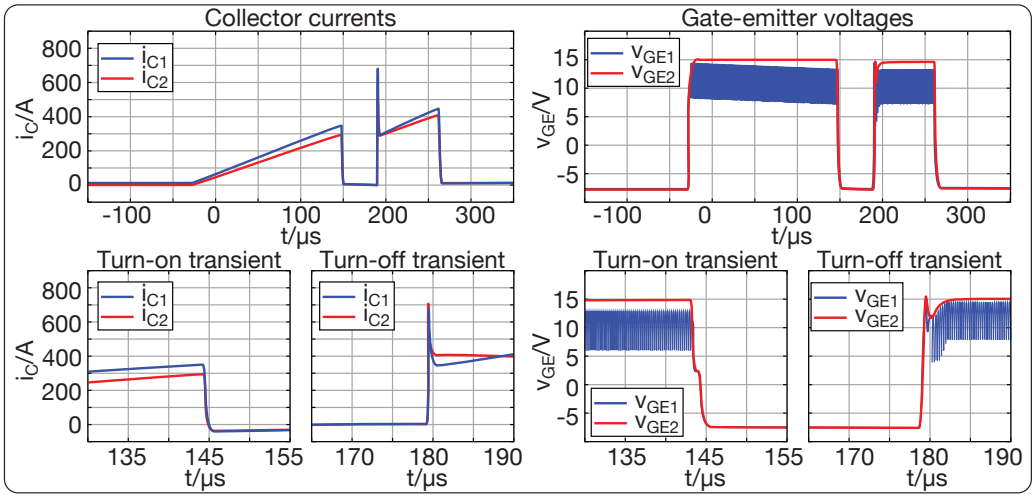
Variable	Value
Test	Double pulse test
2xIGBT	FF650R17IE4 (650 A / 1700 V)
V_{CC}	300 V
I_C	350 A
T_j	25 °C
PWM gate-signal frequency	2 MHz

Fig. 5.15 presents a sequence of waveforms with the closed-loop control algorithm. Each figure shows the collector currents, the gate-emitter voltages and a zoom-in of the turn-on and turn-off transients of the collector currents and gate-emitter voltages.

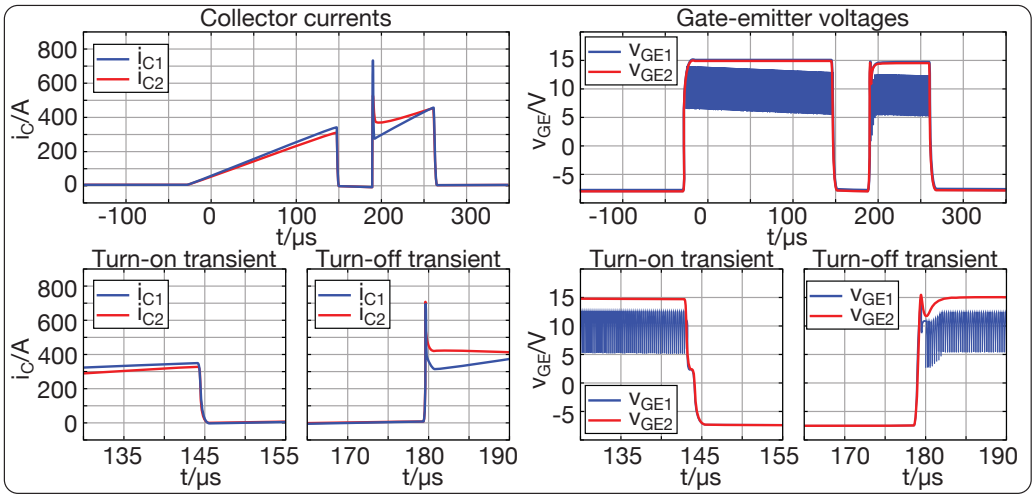
Initially i_{C1} is approximately 387 A and i_{C2} is 286 A after the first current pulse. Both IGBTs have been adjusted to achieve a good dynamic balance. The collector current stationary imbalance reaches approximately 100 A. After 42 steps, which means after 83 IGBT on-states, the gate-emitter voltage of T_1 v_{GE1} is reduced to approximately 13.5 V (mean value). The static imbalance of the collector current is reduced to approximately 53 A after the first current pulse. After 61 steps, the stationary balance of the collector currents is achieved with a IGBT T_1 gate-emitter v_{GE1} equal to approximately 13.3 V (mean value). The imbalance has been reduced to approximately 24 A, which means an imbalance of 7 % according to (5.1) with a total current of 675 A.



(a) Initial condition $i_{C1} - i_{C2} = 101$ A (at the end of the first current pulse).



(b) After 42 steps $i_{C1} - i_{C2} = 53$ A (at the end of the first current pulse).



(c) After 61 steps $i_{C1} - i_{C2} = 24$ A (at the end of the first current pulse).

Figure 5.15: Operation of the closed control loop algorithm for static balancing ($V_{CC} = 300$ V, $i_L = 675$ A, $T_j = 25$ °C).

5.2 FAST SHORT CIRCUIT PROTECTION METHOD (FSCP)

Applications using power converters, particularly high-power applications, typically demand high robustness and reliability. Therefore, fault protection of the semiconductor devices is an important part of the converter protection scheme. This fault protection is required to avoid the destruction of the semiconductor devices during a short circuit situation and, thereby, improve the reliability of the converter. Short circuit can be categorized into two different types:

- Short circuit type I (SCI): The IGBT is turned-on during an existing short circuit in the output circuit (e.g. load).
- Short circuit type II (SCII): A short circuit occurs while the IGBT is conducting.

One of the main features of IGBTs is the capability to limit and to withstand a short circuit for a certain period of time. IGBT designers have to make a compromise between a high short circuit withstand capability and performance during normal operation (e.g. losses). Presently, IGBTs are typically designed to endure a short circuit of maximum duration 10 µs [16], which provides enough time to detect the failure and turn off the device. The short circuit current depends on the turn-on gate-emitter voltage V_{GEon} value and normally amounts to 4. . .6 times the nominal current I_{CN} for common V_{GEon} values, as defined in the short circuit safe operation area SCSOA of the IGBT provided by the manufacturer [66]. For instance, an IGBT with nominal ratings of I_{CN} = 1400 A and a nominal collector-emitter voltage V_{CE} of 1700 V (FF1400R17IP4 from Infineon), is able to withstand a short circuit current of 5600 A for a duration of 10 µs ($4 \times I_{CN}$).

A large variety of short circuit protection schemes have been proposed in the literature, where the most popular scheme is the monitoring of the collector-emitter saturation voltage $V_{CE,sat}$ of the device [16, 38] through high-voltage diodes. However, the measurement of $V_{CE,sat}$ requires a blanking time, which may increase the response time of the short circuit protection system. It can take up to 10 µs to turn off the IGBT during a short circuit. Such a delay causes a drastic rise of the junction temperature T_j of the device. In 1200 V IGBTs the temperature can rise approximately 70 °C during the short circuit, according to the experimental results presented in this section. This causes a high mechanical, thermal and electrical stress of the semiconductor device, which could lead to its destruction.

In recent publications it has been proposed to turn off the IGBT immediately after the detection of the short circuit, in order to achieve a faster response [67]. The short circuit can be detected by measuring the current through the switch, which can be implemented with a Rogowski coil, as presented in [36]. However, turning off the IGBT before the device is desaturated can cause a destruction of the IGBT, since the device is being flooded with carriers. If the IGBT is turned off during this state, the di_C/dt could be higher than the one at the turn-off of a totally flooded IGBT. Thus a higher v_{CE} peak could occur [16].

Another scheme of short circuit protection is based on monitoring the di_C/dt of the current through the switch [68, 69]. An abnormal rate of di_C/dt is used as an indicator of a possible short circuit. The gate will be discharged if a short circuit is detected to reduce the short circuit current through the switch. If another criterion confirms the short circuit, the switch will be turned off, so that the current rise due to the short circuit can be limited. However, in this case the gate may be unnecessarily discharged even if there is no short circuit. This would increase the losses during normal operation.

To summarize, there are reliable short circuit protection schemes for IGBTs available. Nevertheless, a simple and fast detection of the short circuit with a safe turn-off performance and a low-cost implementation is still lacking.

The proposed new method combines fast short circuit detection and a safe turn-off transient, in order to keep the IGBT operating within the SCSOA. This section explains the principle, structure and function of this method along with the experimental results, where the performance is tested in different situations, such as short circuit type I and II.

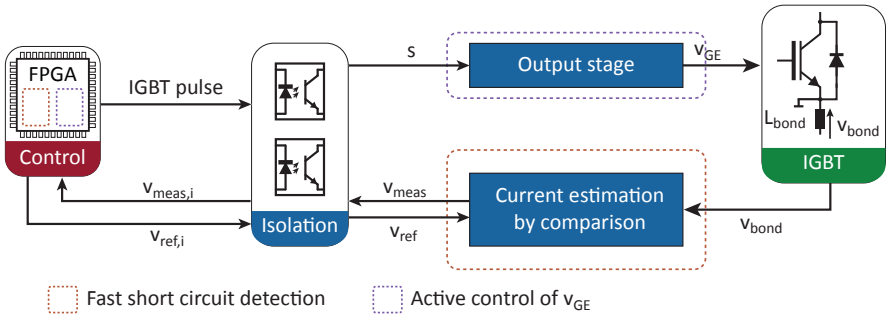


Figure 5.16: Block diagram of the fast short circuit protection scheme.

5.2.1 Principle of the fast short circuit protection method

The new protection scheme is divided into two main stages, see Fig. 5.16:

1. Fast short circuit detection: The short circuit is detected using an algorithm that distinguishes between the short circuit types I and II. The current is estimated with the CEC method presented in Section 3.1.2.
2. Active control of the gate-emitter voltage v_{GE}: After the short circuit detection, the gate-emitter voltage is decreased in order to reduce the short circuit collector current and to accelerate the desaturation of the IGBT.

5.2.2 Fast short circuit detection

In this scheme, the collector current is estimated with the method presented in Section 3.1.2, which is based on the measurement of the voltage v_{bond} across the stray inductance L_{bond}. An algorithm detects if the IGBT is in a short circuit condition. This method allows a simple and fast estimation of the collector current for short circuit detection. Moreover, the algorithm can distinguish between short circuits of type I and II.

The algorithm calculates the time interval $t_{\text{meas,i-on}}$, defined in Fig. 3.5 of Sec. 3.1.2, during the turn-on transient of the IGBT. If the interval $t_{\text{meas,i-on}}$ is longer than a predefined value, this means that the collector current has reached an abnormally high value (e.g. $I_{\text{C}} > 2 \times I_{\text{CN}}$) which is considered a short circuit type I (SCI) of the IGBT.

If during the on-state of the IGBT the algorithm detects a high value from the current estimation scheme and the calculated $t_{\text{meas,i-on}}$ is longer than a predefined value (e.g. $t_{\text{meas,i-on}} > 100\,\text{ns}$ for the investigated (1400 A / 1200 V) IGBT FF1400R12IP4), the collector current has an undergone an abnormal increase during the on-state of the IGBT, and the algorithm determines that the IGBT is in a short circuit type II (SCII). After the detection of short circuits (SCI or SCII) the algorithm proceeds with the turn-off strategy.

Fig. 5.17 shows a simplified flow diagram of the short circuit detection scheme. The trigger signal is defined as s (e.g. PWM), and the status signals for the SCI routine and the SCII routine are defined as *SCIs* and *SCIIs* respectively. The internal counter for the SCI routine is defined as k_{SC1} and for the SCII routine is defined as k_{SC2}. The variables r_{SC1} and r_{SC2} are the limits of the counters k_{SC1} and k_{SC2} respectively, which define the intervals necessary to determine if a SCI or SCII occurs.

At the begin of the algorithm, the short circuit status signals *SCIs*, *SCIIs* and the counters k_{SC1}, k_{SC2} are set to zero. The algorithm operates as follows:

Short circuit type I routine:

1. When a low to high transient of the trigger signal *s* is detected, a timer *t* starts and if the timer *t* is longer than a predefined value (e.g. $t > 2\,\mu s$; the maximal necessary time to turn-on the investigated IGBT), the IGBT has been already turned on, therefore the SCII routine is activated.
2. If $t < 2\,\mu s$, the IGBT is in the turn-on process. When a low to high transient of $v_{meas,i\text{-}on}$ is detected, the SCI counter k_{SC1} is made to start counting.
3. The counter k_{SC1} keeps counting as long as $v_{meas,i\text{-}on}$ is 1.
4. If the counter k_{SC1} exceeds the reference limit value r_{SC1}, a SCI is detected and *SCIs* changes to 1. If the reference limit value r_{SC1} has not been exceeded and $v_{meas,i\text{-}on}$ changes its status to zero, the SCII routine is activated.

Short circuit type II routine:

5. If the trigger signal *s* changes to zero the algorithm returns to the SCI routine (step 1), because the IGBT is being turned off.
6. If a low to high transition of $v_{meas,i\text{-}on}$ is produced while *s* is still high, the SCII counter k_{SC2} is made to start counting.
7. The counter k_{SC2} keeps counting as long as $v_{meas,i\text{-}on}$ is 1.
8. If the counter k_{SC2} exceeds the reference limit value r_{SC2}, a SCII is detected and *SCIIs* is set to 1. If the reference limit value r_{SC2} has not been exceeded and $v_{meas,i\text{-}on}$ change its status to zero, the algorithm returns to the step 5.

Fig. 5.18 shows the signal $v_{meas,i\text{-}on}$ during SCI and SCII. The reference limit value r_{SC1} can be obtained by measuring $t_{meas,i\text{-}on}$ when the collector current is $I_C = 2 \times I_{CN}$. This test should be carried out during the protection scheme initialization phase. In an industrial converter this test could e.g. be integrated into a start-up routine of the converter. During the conduction state of the IGBT the rate of change of the collector current is usually limited by the load inductance. Therefore, a quick rise of the collector current (high di_C/dt) is an indicator of a SCII. The reference limit value for the SCII routine r_{SC2} can be much lower than the reference limit for the SCI routine r_{SC1}. In this case, r_{SC2} is set close to zero (e.g. 100 ns for the (1400 A / 1200 V) IGBT FF1400R12IP4).

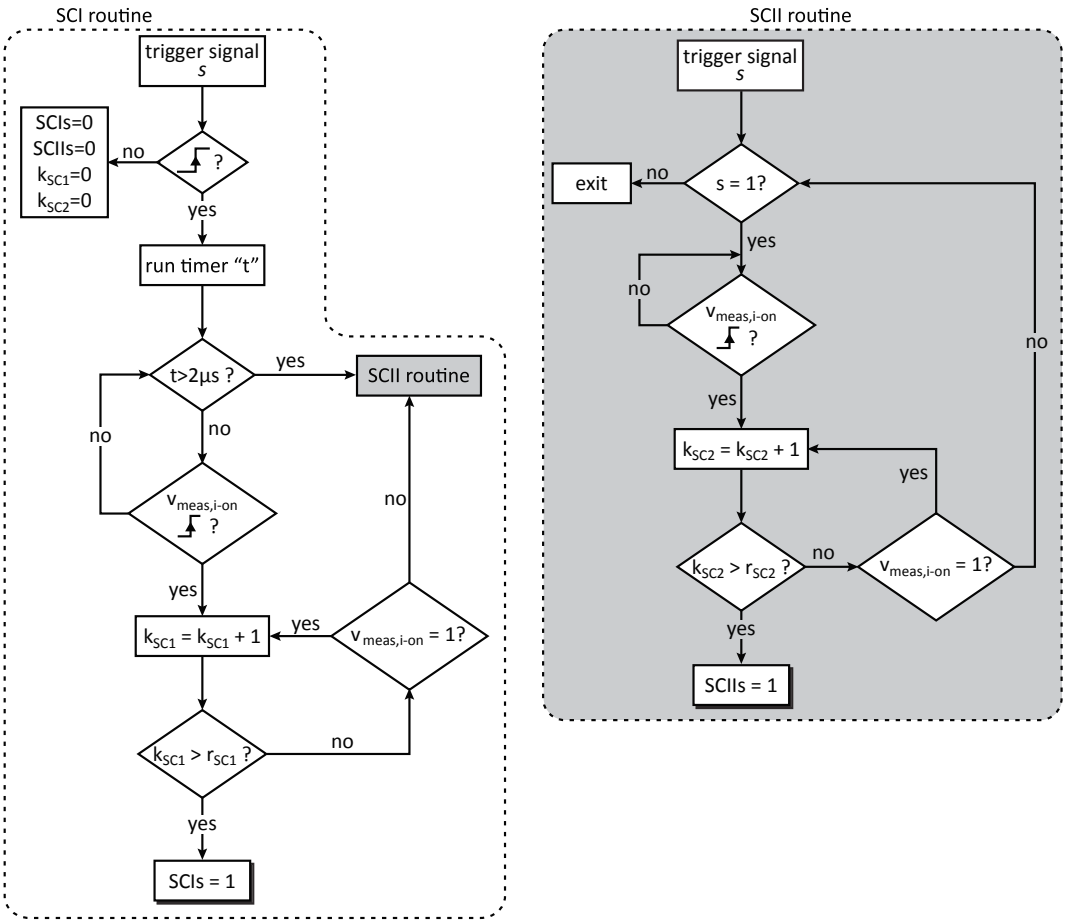


Figure 5.17: Block diagram of the algorithm for fast short circuit protection.

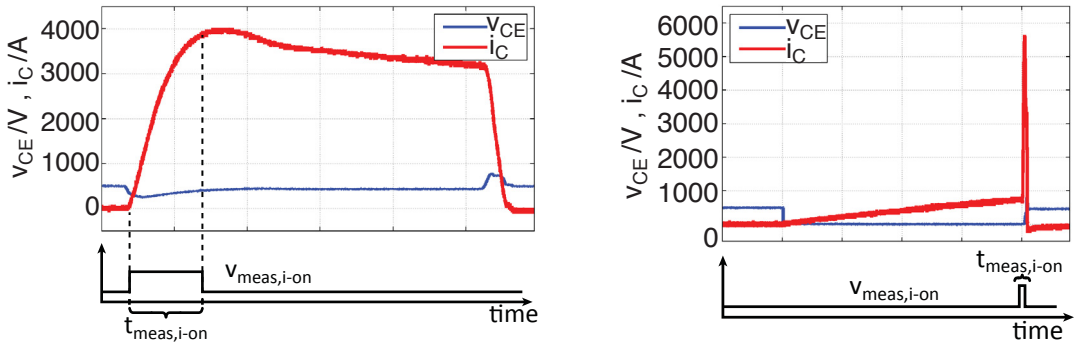


Figure 5.18: Collector current and $v_{\text{meas,i-on}}$ signal during short circuits (V_{CC} = 500 V, T_{j} = 25 °C). (a) SCI (2µs/div), and (b) SCII (50µs/div).

5.2.3 Active control of the gate-emitter voltage

Actions after the detection of the short circuit vary depending on the type of the short circuit. In case of a SCI, the IGBT can be turned off immediately after the detection of the short circuit. However, in the case of a SCII, the IGBT must be desaturated before it is turned off [16].

To achieve a faster desaturation of the IGBT during such a short circuit event and to reduce the junction temperature rise, the corresponding short circuit current could be decreased by a

moderate reduction of the gate-emitter voltage v_{GE} after the short circuit has been detected.

In principle an analog implementation can be used. However, such a solution could be expensive. One alternative solution is a gate unit featuring three voltages levels of V_{GEon1}, V_{GEon2} and V_{GEoff1} (e.g. $V_{GEon1} = +15\,V$, $V_{GEon2} = +11\,V$ and $V_{GEoff1} = -15\,V$) for the output stage. In this case the output stage must be able to command the gate terminal with the output stage voltage levels V_{GEon1}, V_{GEon2} and V_{GEoff1} which could be generated by the power supply of the GDU. The basic structure of this realization is shown in Fig. 5.19. A further realization possibility for the v_{GE} reduction is the modulation of the trigger gate signal. The internal capacitances of the IGBT together with the gate resistances behave as an *RC* low-pass filter, as seen in Fig. 5.20. The cut-off frequency of the filter ($\sim$2 Mhz for the (1400 A / 1200 V) IGBT FF1400R12IP4), depends on the capacitances C_{GE}, C_{CG} and the total gate resistance $R_{G,tot} = R_G + R_{G,int}$.

One possible implementation of the output stage is presented in Fig. 5.21. The IGBT is triggered by the signal *s*. Fig. 5.22 shows an example of the reduction of the gate-emitter voltage v_{GE} based on a pulse-width modulated trigger gate signal *s*. At instant t_2 a short circuit has been detected and the trigger signal *s* starts being pulse-width modulated at a high frequency. The carrier frequency should be sufficiently above the cut-off frequency of the low-pass filter in order to reduce the high frequency content of the gate-emitter voltage. This scheme provides a fast reduction of the gate-emitter voltage v_{GE}.

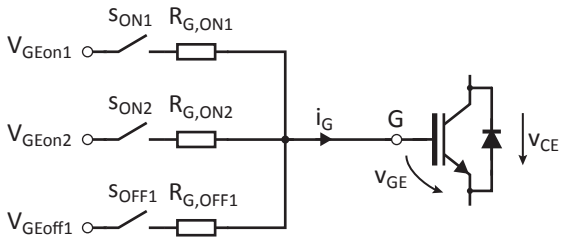


Figure 5.19: Equivalent circuit of a GDU with fast short circuit protection and three power supply voltages.

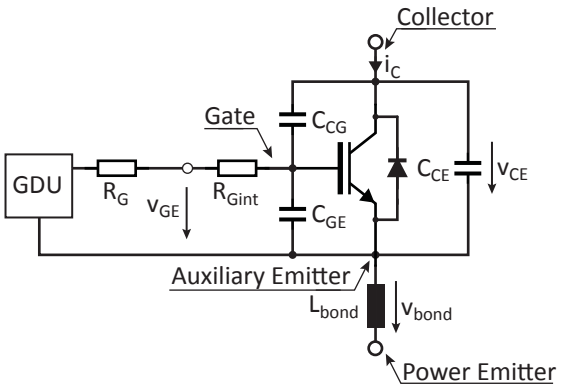


Figure 5.20: Representation of a simplified model of an IGBT.

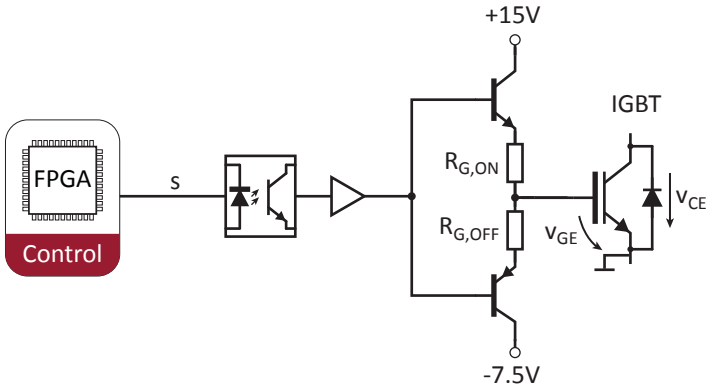


Figure 5.21: Possible implementation of a GDU output stage for fast short circuit protection.

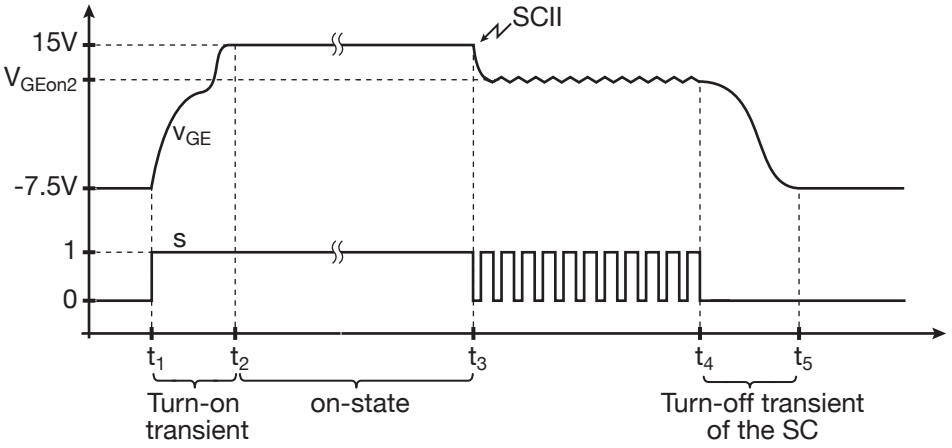


Figure 5.22: Principle of active control of the gate-emitter voltage v_{GE} for fast short circuit protection in case of SCII.

5.2.4 Experimental verification

5.2.4.1 Test description

The fast short circuit protection method has been tested in a buck converter, as shown alongside circuit configurations for SCI and SCII in Fig. 5.23. A SCI is produced by bypassing the upper IGBT. A SCII is produced by turning on the upper IGBT for 8 µs while the lower IGBT is in the on-state. The test conditions are listed in Table 5.3.

Table 5.3: Test conditions for the verification of the fast short circuit detection scheme

Variable	Value
IGBT	FF1400R12IP4 (1400 A / 1200 V)
V_{CC}	100...500 V
T_j	25 °C
PWM gate-signal frequency	2 MHz

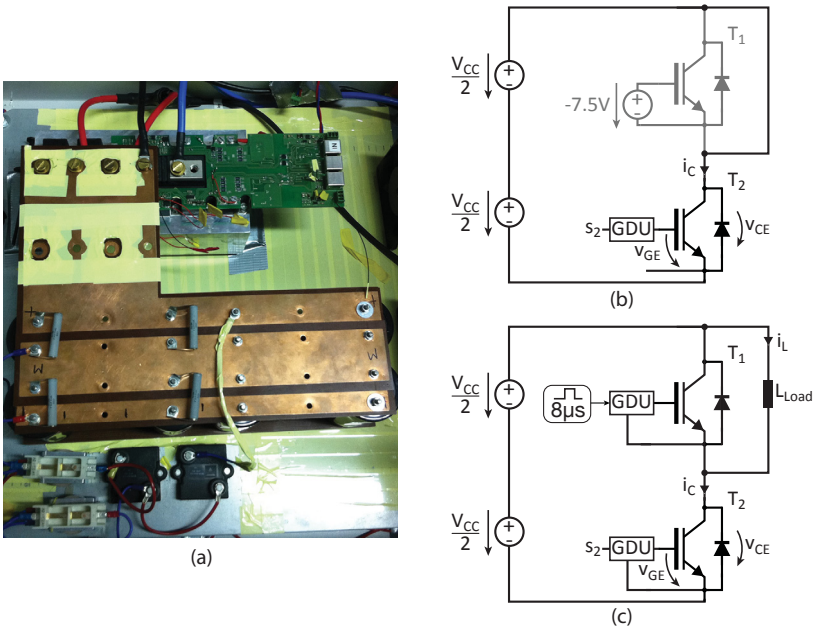


Figure 5.23: Setup used for the verification of the fast short circuit protection scheme. (a) Photography, circuit configuration for (b) SCI, and (c) SCII.

5.2.4.2 Experimental results

Figure 5.24 shows measurement results of a SCI with different gate-emitter voltages v_{GE}. With the standard $V_{CE,sat}$ detection method in combination with a soft turn-off of the short circuit current, the IGBT is turned off after 10 µs, reaching a collector current of 4000 A. However, with the new method, the collector current during the short circuit was reduced by 50% when the gate-emitter voltage v_{GE} is decreased from 15 V to 11.2 V. In this case the IGBT was turned off 3 µs after the detection of the short circuit. This time had been previously set in the FPGA.

The power, energy and junction temperature during the short circuit are shown in Fig. 5.25. The junction temperature T_j is calculated with the adiabatic model of the IGBT provided by the manufacturer, shown in (5.2), where A is a constant relating to the thermal model. Assuming a junction temperature of 80 °C before the SCI, the temperature rises to 150 °C when the standard $V_{CE,sat}$ detection method and soft turn-off is used. With the active control of the gate-emitter voltage v_{GE}, the junction temperature T_j rises around 15 °C at a gate-emitter voltage of v_{GE} = 11.2 V, reaching a junction temperature of 95 °C. The losses were reduced by more than 60% compared to the losses when the conventional $V_{CE,sat}$ detection method and soft turn-off is used. When the IGBT is turned off immediately after the detection (described as "without delay" in Fig. 5.24, Fig. 5.25), the junction temperature rises around 5 °C, reaching a junction temperature of only 85 °C.

$$T(t) = \frac{1}{A}\int_0^t P(t)dt \tag{5.2}$$

Experimental results for SCII are shown in Fig. 5.26. The collector current reaches 6 kA during the short circuit. If the gate-emitter voltage is reduced to v_{GE} = 12 V after the detection of the short circuit, the IGBT is turned off with a short circuit collector current of approximately 3 kA. When v_{GE} is reduced to 11.2 V, the IGBT collector current is further reduced to approximately 2.2 kA. It should be mentioned that the proposed new scheme allows safe turn-off performance and keeps the IGBT operating within the SCSOA.

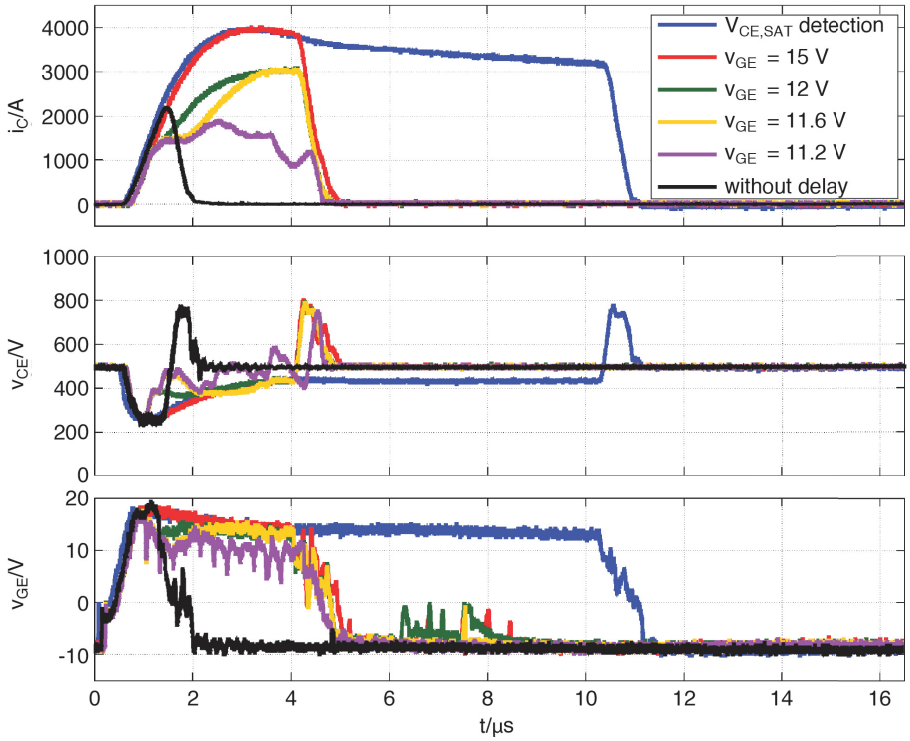


Figure 5.24: Collector current, collector-emitter voltage and gate-emitter voltage for short circuit type I using active control of the gate-emitter voltage v_{GE} (IGBT = FF1400R12IP4, V_{CC} = 500 V, T_j = 25°C).

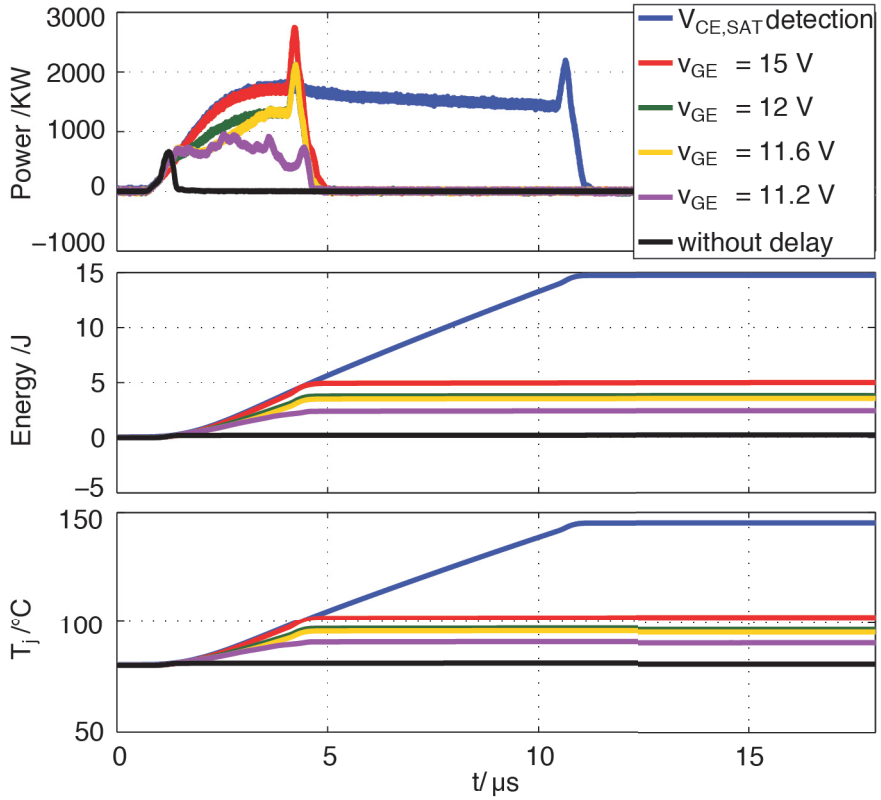
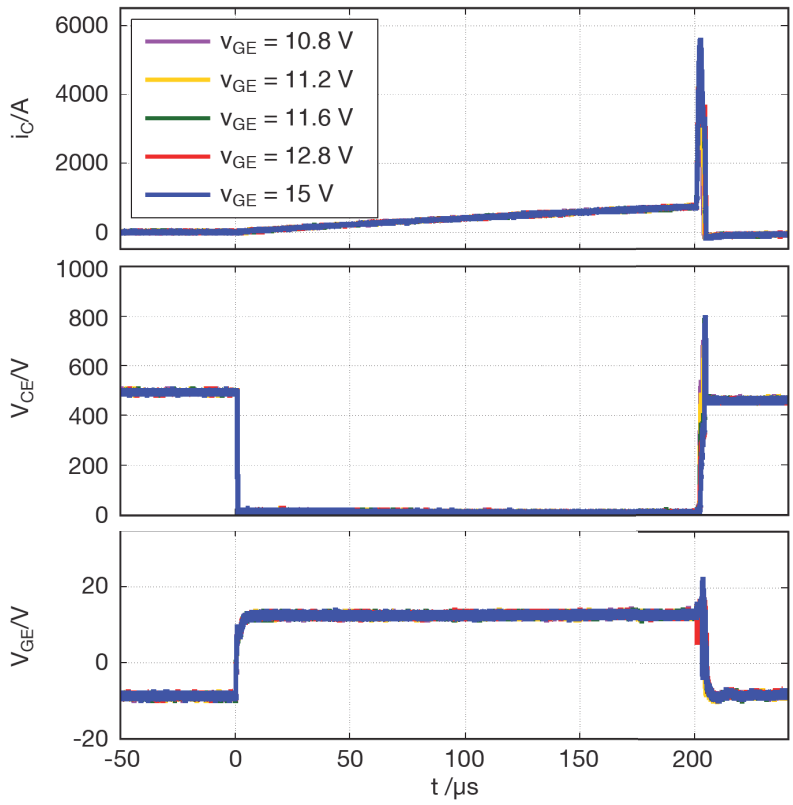
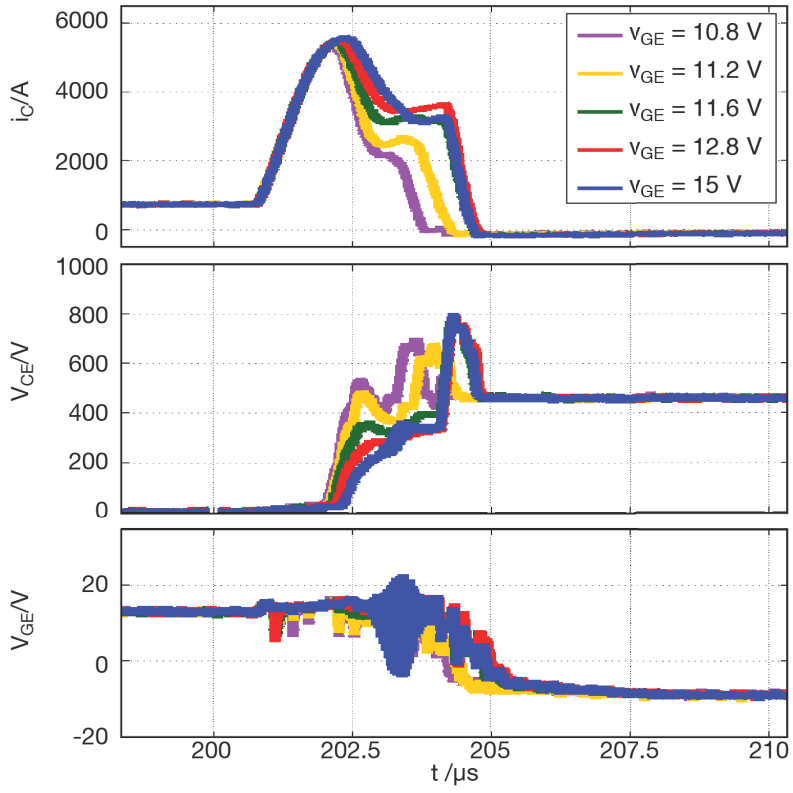


Figure 5.25: Instantaneous power, loss energy and T_j during a SCI with active control of the gate-emitter voltage v_{GE} (V_{CC} = 500 V, T_j = 25°C).



(a)



(b)

Figure 5.26: Collector current, collector-emitter voltage and gate-emitter voltage for short circuit type II using active control of the gate-emitter voltage v_{GE} (V_{CC} = 500 V, I_C = 1200 A, T_j = 25°C). (a) Entire test time and (b) zoom-in on the short circuit instant.

5.3 NEW SWITCHING LOSS REDUCTION SCHEME (SLR)

In conventional commercially available GDUs, IGBTs are usually turned on and turned off by connecting that IGBT gate terminal to a positive or negative GDU power supply voltage (V_{GEon} = +15 V, V_{GEoff} = −15 V) via turn-on and turn-off gate resistance $R_{G,ON}$ and $R_{G,OFF}$. In order to improve the switching behaviour of IGBTs, several authors have propose the implementation of gate drivers which can control the di_C/dt and dv_{CE}/dt during the turn-on and turn-off transients and dynamically adjust the gate current to the switching phases of the IGBT. The most common implementations are:

- Active modification of several gate resistances e.g. [70–73]
- Current source gate current shaping e.g. [74–77]
- Voltage source gate-emitter voltage shaping e.g. [78–81]

In some of these solutions, a closed-loop control scheme for di_C/dt or dv_{CE}/dt is implemented by measuring the collector current with a shunt resistor, Rogowski coil or by indirect measurement of di_C/dt by means of the stray inductance of the IGBT modules [73, 81]. The collector-emitter voltage v_{CE} can be measured with a compensated voltage divider or with a small capacitor in order to sense the dv_{CE}/dt directly.

One of the disadvantages of these solutions are their expensive measurement methods, the use of fast analog-to-digital converters [77] and the implementation of an analog controller, which reduces the flexibility of the system. Another disadvantage is the limited maximum charge rate of the controlled di_C/dt or dv_{CE}/dt.

5.3.1 Principle of the new switching loss reduction scheme (SLR)

An IGBT model including different switching phases is presented in Fig. 5.27. The turn-on transient interval occurs between $t_0 < t < t_3$ while the turn-off transient is between $t_4 < t < t_7$. The different phases of an IGBT turn-on and turn-off transients have been discussed extensively in the literature (e.g. [6, 7, 9, 16]). Below, the different phases are discussed briefly as a basis for the description of the proposed switching scheme.

Turn-on transient phases

Phase 1 ($t_0 < t < t_1$): The gate current i_G charges the input capacitances C_{GE} and C_{GC}. The gate-emitter voltage v_{GE} rises to the threshold voltage $V_{GE,th}$ with a time constant determined by $\approx(R_{G,ON} + R_{G,int})\cdot(C_{GE} + C_{GC})$. During this period, i_C and v_{CE} do not change. The turn-on delay ($t_1 - t_0$) can be decreased by reducing the gate turn-on resistance $R_{G,ON}$.

Phase 2 ($t_1 < t < t_2$): v_{GE} has exceeded $V_{GE,th}$, and i_C increases approximately proportionally to the rise of v_{GE}. The di_C/dt can be controlled by $R_{G,ON}$. The maximum allowable di_C/dt is limited by the IGBT technology, the RRSOA of the diode, the interface between GDU and IGBT and/or EMI.

Phase 3 ($t_2 < t < t_3$): v_{GE} remains at a constant voltage V_m (Miller effect) and v_{CE} starts decreasing. The dv_{CE}/dt can be adjusted with $R_{G,ON}$. To reduce the turn-on losses, v_{CE} should decrease fast, which can be achieved by reducing $R_{G,ON}$. After t_3, v_{GE} increases to 15 V.

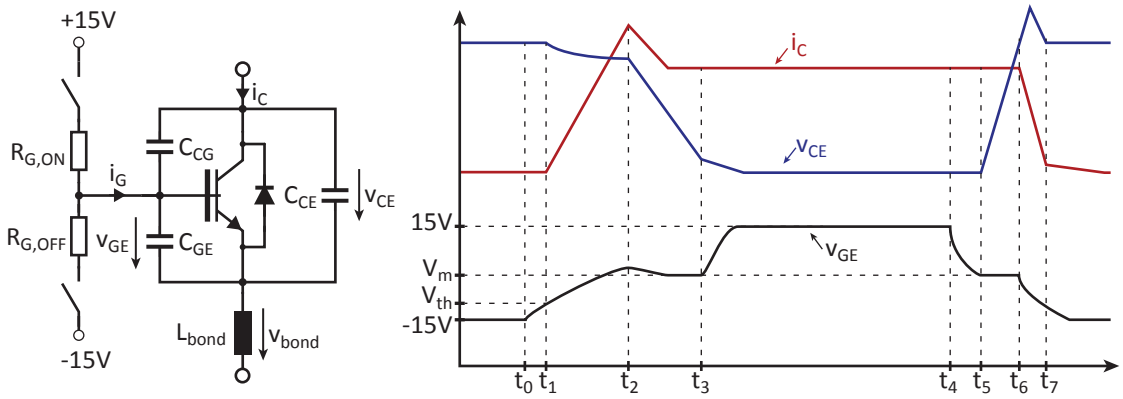


Figure 5.27: IGBT model and switching transient during the turn-on and turn-off of the IGBT.

Turn-off transient phases

Phase 4 ($t_4 < t < t_5$): v_{GE} decreases to V_m with a time constant determined by $\approx(R_{G,OFF} + R_{G,int})\cdot(C_{GE} + C_{GC})$. The turn-off delay ($t_5 - t_4$) can be decreased by reducing the gate turn-off resistance $R_{G,OFF}$, so that the absolute value of the negative gate current is increased and v_{GE} reaches V_m rapidly.

Phase 5 ($t_5 < t < t_6$): v_{GE} remains at a constant voltage V_m and v_{CE} starts rising. The dv_{CE}/dt can be adjusted by $R_{G,OFF}$. To reduce the turn-off losses, $R_{G,OFF}$ should be decreased so that v_{CE} can reach the dc-link voltage V_{CC} rapidly.

Phase 6 ($t_6 < t < t_7$): v_{CE} has reached V_{CC} and i_C decreases approximately proportionally to v_{GE}. The di_C/dt can be adjusted by $R_{G,OFF}$ to regulate the turn-off over-voltage peak in the IGBT.

In most conventional GDUs, an IGBT is turned on and off with fixed voltages (e.g. $V_{GEon} = +15\,V$, $V_{GEoff} = -15\,V$) and gate resistances ($R_{G,ON}$ and $R_{G,OFF}$). Moreover, a large part of these are generated during the phases where v_{GE} is equal to V_m, namely phase 3 ($t_2 < t < t_3$) for the turn-on and phase 5 ($t_5 < t < t_6$) for the turn-off transient. Therefore, the switching losses can be reduced by increasing the absolute value of the gate current in these phases so that the absolute value of the occurring dv_{CE}/dt is increased.

The proposed scheme provides a dynamic variation of the gate current with an active selection of the gate resistances in the switching phase 3 and phase 5, which are detected with the voltage across the stray inductance L_{bond}. A block diagram of the GDU is shown in Fig. 5.28, which has two main stages:

a) Output stage with two gate turn-on and turn-off resistances: recharges the IGBT input capacitances with gate resistances which are adjusted according to the switching phases.

b) Switching phase detection: detects the switching phase with the information given by the method *current estimation by comparison (CEC)* [40] presented in Section 3.1.2.

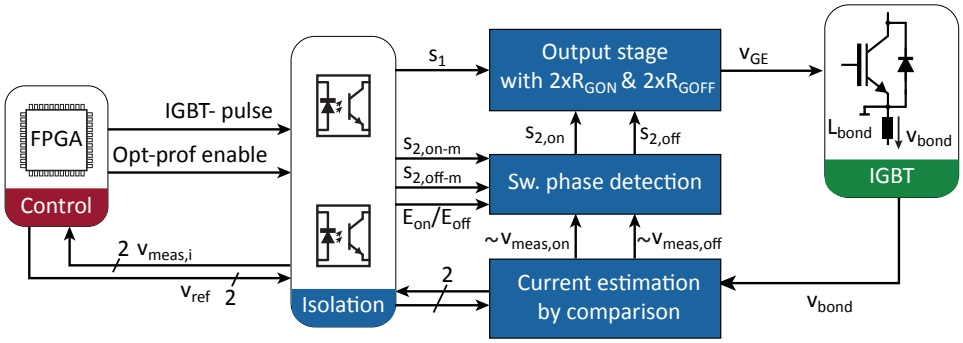


Figure 5.28: Block diagram of the concept of the optimal switching profile scheme.

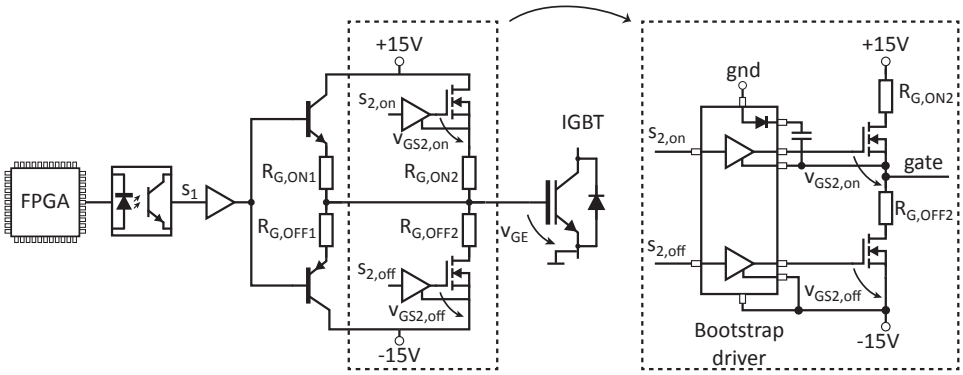


Figure 5.29: GDU prototype output stage with two different gate turn-on and gate turn-off resistances.

5.3.1.1 Output stage with two gate resistances for turn-on and turn-off transients

The gate current is adjusted by an active connection or disconnection of gate resistances in parallel during the switching transient of the IGBT. A scheme for this implementation is shown in Fig. 5.29. The digital signal s_1 turns an IGBT on and off with standard gate resistances $R_{G,ON1}$ and $R_{G,OFF1}$.

The total gate-on and gate-off resistances are dynamically modified by connecting gate resistances $R_{G,ON2}$ and $R_{G,OFF2}$ in parallel to $R_{G,ON1}$ and $R_{G,OFF1}$ respectively. These are controlled by the digital signals $s_{2,on}$ and $s_{2,off}$, given by the *switching phase detection* stage. The value of $R_{G,ON2}$ and $R_{G,OFF2}$ is close to zero, e.g. 0.2 Ω. A bootstrap driver with independent input signals is used to control the MOSFETs of the push-pull amplifier. This scheme also allows the output stage to be manually controlled by the central control unit.

5.3.1.2 Switching phase detection

The switching phases are detected with the method *current estimation by comparison (CEC)* [40], presented in Section 3.1.2, with a modification of the reference voltages. The CEC scheme and the ideal waveforms during the switching transient of the collector current i_C, the voltage across the stray inductance v_{bond} and the output of the comparators are shown in Fig. 5.30.

The binary signals $\sim v_{meas,on}$ and $\sim v_{meas,off}$ are generated by the CEC stage, where, in this case, a low value indicates whether the collector current is increasing (turn-on transient, $\sim v_{meas,off} = 0$)

or decreasing (turn-off transient, $\sim v_{\text{meas,on}} = 0$). The switching phases can be detected according to the state of the output signals from the CEC, the enable signals $E_{\text{n,on}}$ and $E_{\text{n,off}}$ and the trigger signal s_1 as presented in Table 5.4, where the signals s_1, $E_{\text{n,on}}$ and $E_{\text{n,off}}$ are provided by the FPGA. The enable signals $E_{\text{n,on}}$ and $E_{\text{n,off}}$ also allow for control of the trigger signals for the output stage of the SLR $s_{2,\text{on}}$ and $s_{2,\text{off}}$ by the switching phase detection stage or by the FPGA through the signals $s_{2,\text{on-m}}$ and $s_{2,\text{off-m}}$ (manual control).

Table 5.4: Switching phase detection

s_1	$E_{\text{n,on}}$	$E_{\text{n,off}}$	$\sim v_{\text{meas,on}}$	$\sim v_{\text{meas,off}}$	Switching phase
0	0	0	1	1	IGBT in off-state
1	1	0	1	1	Phase 1 ($t_0 < t < t_1$)
1	1	0	1	0	Phase 2 ($t_1 < t < t_2$)
1	1	0	0	1	Phase 3 ($t_2 < t < t_3$)
1	0	0	1	1	IGBT in on-state
0	0	1	1	1	Phase 4 and phase 5 ($t_4 < t < t_6$)
0	0	1	0	1	Phase 6 ($t_6 < t < t_7$)

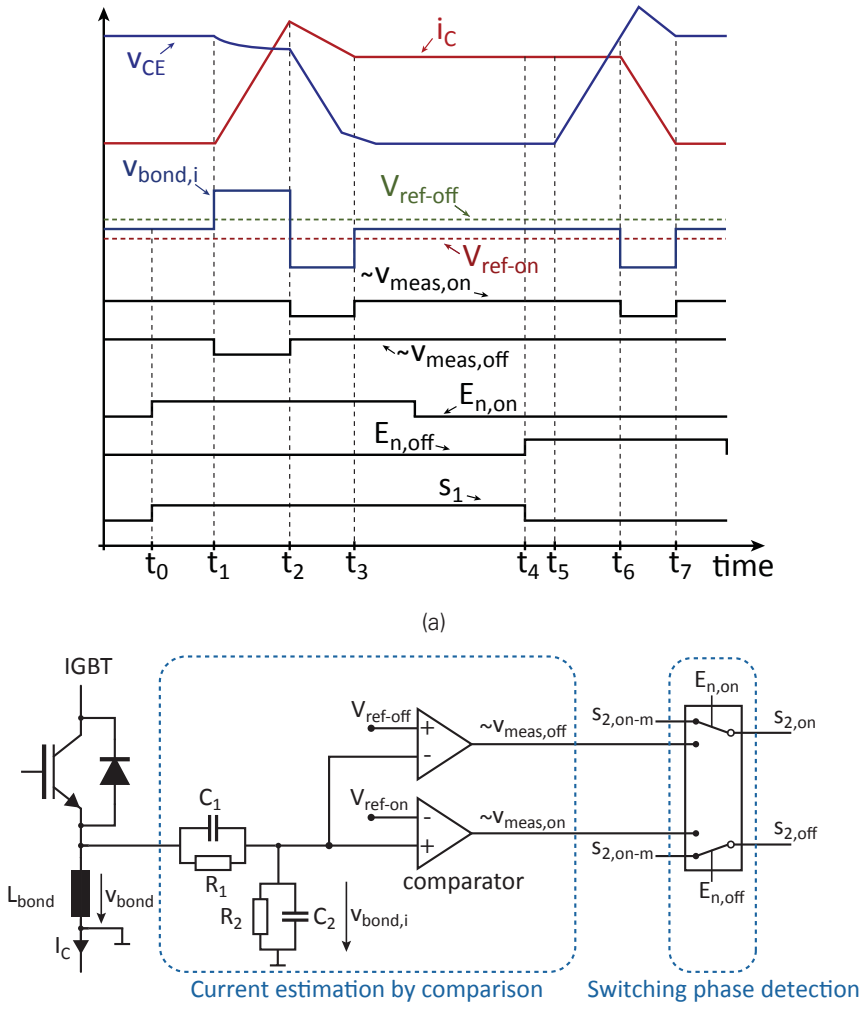


Figure 5.30: Switching phase detection scheme. (a) Ideal waveforms, and (b) possible implementation.

During the turn-on transient, the digital signal $E_{n,on}$ enables the connection of $\sim v_{meas,off}$ with $s_{2,on}$ which triggers the parallel connection of the gate turn-on resistances $R_{G,ON2}$ with $R_{G,ON1}$. During the turn-off transient, the digital signal $E_{n,off}$ enables the connection of $\sim v_{meas,on}$ with $s_{2,off}$ which triggers the parallel connection of the gate turn-off resistances $R_{G,OFF2}$ with $R_{G,OFF1}$. The switching conditions during each stage are summarized in Table 5.5.

Table 5.5: Optimal switching profile conditions

Time	Phase detection	Gate resistance	Effect
Turn-on transient:			
Phase 1 ($t_0 - t_1$)	$\sim v_{meas,off} = 1$	$R_{G,ON} = R_{G,ON1} \parallel R_{G,ON2}$	Turn-on delay is reduced.
Phase 2 ($t_1 - t_2$)	$\sim v_{meas,off} = 0$	$R_{G,ON} = R_{G,ON1}$	di_C/dt adjustment, IGBT is turned on with defined di_C/dt.
Phase 3 ($t_2 - t_3$)	$\sim v_{meas,off} = 1$	$R_{G,ON} = R_{G,ON1} \parallel R_{G,ON2}$	dv_{CE}/dt adjustment, v_{CE} rapidly decreases and turn-on switching losses are reduced.
Turn-off transient:			
Phase 4 ($t_4 - t_5$)	$\sim v_{meas,on} = 1$	$R_{G,OFF} = R_{G,OFF1} \parallel R_{G,OFF2}$	Turn-off delay is reduced.
Phase 5 ($t_5 - t_6$)	$\sim v_{meas,on} = 1$	$R_{G,OFF} = R_{G,OFF1} \parallel R_{G,OFF2}$	dv_{CE}/dt adjustment, v_{CE} rapidly increases and turn-off switching losses are reduced.
Phase 6 ($t_6 - t_7$)	$\sim v_{meas,on} = 0$	$R_{G,OFF} = R_{G,OFF1}$	di_C/dt adjustment, IGBT is turned off with defined di_C/dt and the over-voltage peak can be adjusted.

5.3.2 Experimental verification

A GDU lab setup has been designed and built in order to test the derived switching loss reduction schemes (SLR). Fig. 5.31 shows the new GDU with the following features:

- Output stage with two gate turn-on and gate turn-off resistances.
- Current estimation by comparison (CEC) method.
- Switching phase detection.
- Trigger signals for the output stage of the SLR $s_{2,on}$ and $s_{2,off}$ are provided by the switching phase detection stage or by the FPGA through the signals $s_{2,on\text{-}m}$ and $s_{2,off\text{-}m}$ (manual control).

5.3.2.1 Test description

The proposed new scheme was tested in a buck converter as shown in Fig. 5.32. The test conditions are listed in Table 5.6. Due to the large value of the internal gate resistance $R_{G,int}$ (2.25 Ω),

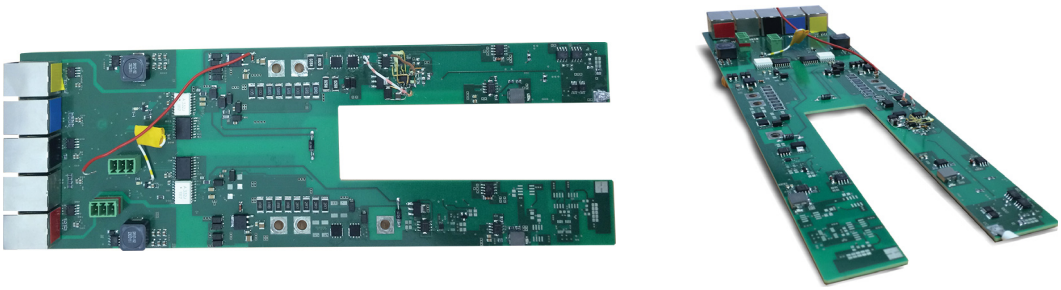


Figure 5.31: Lab setup GDU PCB for switching loss reduction (SLR).

Table 5.6: Basic values of the buck converter and GDU for the investigation

Variable	Value	Description
IGBT	1400 A / 1700 V	Fuji:2MBI1400VXB-170E-50
V_{CC} V_{CC}	100...700 V	DC-Link voltage
i_C	100...1400 A	Collector current
L_{Load}	25.3 μH	Inductive load
C_1	2.8 mF	DC-Link capacitance
T_j	25 and 125 °C	Junction temperature
V_{GEon}	+15 V	Turn-on gate-emitter voltage
V_{GEoff}	−15 V	Turn-off gate-emitter voltage
$R_{G,int}$	2.25 Ω	Internal gate resistance
$R_{G,ON1}$	2 Ω	External gate turn-on resistance 1
$R_{G,ON2}$	0.2 Ω	External gate turn-on resistance 2
$R_{G,OFF1}$	1.7 Ω	External gate turn-off resistance 1
$R_{G,OFF2}$	0.2 Ω	External gate turn-off resistance 2

the external gate turn-on and off resistances ($R_{G,ON1}$ and $R_{G,OFF1}$) were increased from 0.47 Ω and 0.68 Ω (datasheet values) to 2 Ω and 1.7 Ω for the investigation, respectively. Thus, the total gate turn-on resistance when $R_{G,ON2}$ is connected in parallel, is reduced from 4.25 Ω (2 Ω + 2.25 Ω) to 2.45 Ω (0.2 Ω+2.25 Ω). During the turn-off transient, the total gate turn-off resistance when $R_{G,OFF2}$ is connected in parallel, is reduced from 3.95 Ω (1.7 Ω + 2.25 Ω) to 2.45 Ω (0.2 Ω+2.25 Ω). Thus, the gate current features a significantly larger variation by the parallel connected gate resistances and, in turn, the function and the principle of the new method can be better verified.

5.3.2.2 Experimental results

A comparison of the results obtained with a conventional GDU (+15 V, −15 V, $R_{G,ON}$, $R_{G,OFF,D}$) and a GDU with the switching loss reduction scheme SLR are shown in Fig. 5.33. The blue lines for i_C, v_{CE}, $P_{ON,T}$ and $W_{ON,T}$ represent the collector current, collector-emitter voltage, power and energy switching waveforms, respectively, during the turn-on transient with a conventional GDU with a total gate turn-on resistance $R_{G,ON} + R_{G,int} = 4.25\,\Omega$. The results plotted with a red line have been obtained when the trigger signals for the output stage of SLR are sent by the FPGA, which operates by reducing the total gate turn-on resistance to 2.45 Ω after a manually predefined time. The results plotted with a green line have been obtained with the automatic turn-on method, where the reduced gate turn-on resistance (R_{GON2}) is triggered by the signal $\sim v_{meas,off}$.

The automatic turn-on method increases the di_C/dt by approximately 40% compared to a conventional GDU. Moreover, the collector-emitter voltage variation (dv_{CE}/dt) has been approximately doubled, which entails a reduction of the turn-on losses $W_{ON,T}$ by 37%.

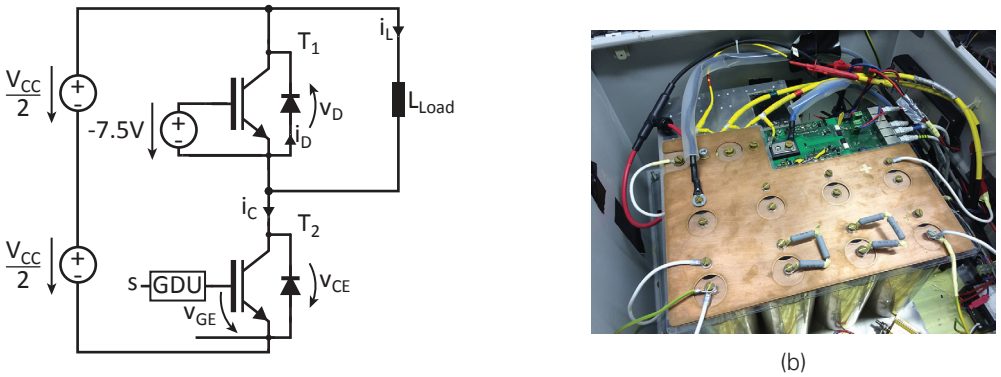


Figure 5.32: Test setup for the switching loss reduction investigation. (a) Converter circuit, and (b) photograph of the buck converter.

The gate signals of the automatic turn-on method are shown in Fig. 5.34. In the time interval 2 µs < t < 3.2 µs, the IGBT is turned on with a reduced gate turn-on resistance by connecting $R_{G,ON2}$ in parallel. The turn-on delay is reduced by around 1 µs. In the time interval 3.2 µs < t < 3.5 µs $R_{G,ON2}$ is disconnected (total $R_{G,ON}$ = 4.25 Ω) in order to turn on the IGBT with a defined di_C/dt (datasheet value). After t = 3.5 µs , $R_{G,ON2}$ is again connected in parallel in order to increase the dv_{CE}/dt and to reduce v_{CE} rapidly.

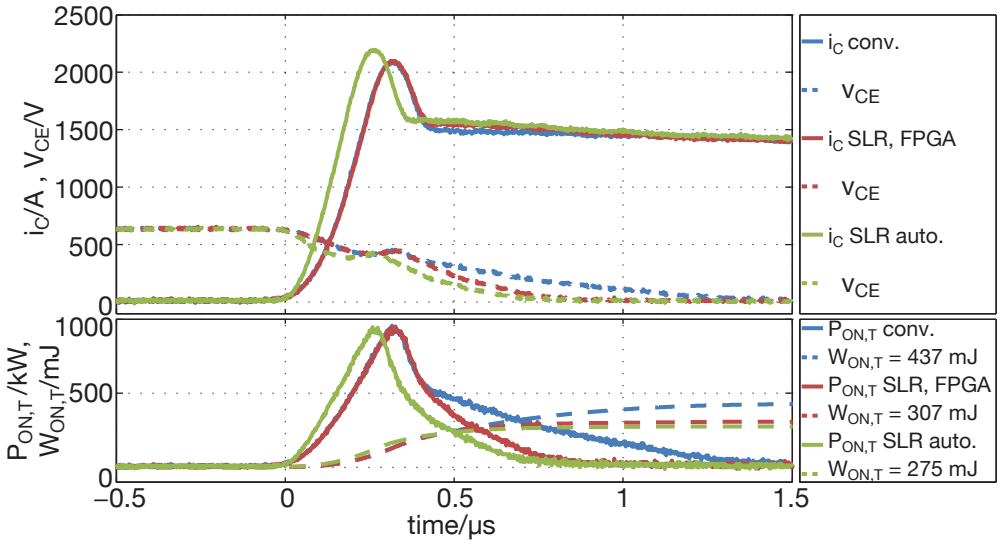


Figure 5.33: Collector current and energy losses during the turn-on transient of the IGBT for different switching profiles (V_{CC} = 650 V, I_C = 1400 A, T_j = 25 °C).

Fig. 5.35 shows the turn-off transient of the IGBT with a conventional GDU and one using the SLR scheme. With the automatic turn-off method, the turn-off delay is reduced by approximately 150 ns, the dv_{CE}/dt is increased by approximately 48%, the $|di_C/dt|$ is increased by 20%, and the turn-off losses $W_{OFF,T}$ are reduced by approximately 21 % compared to the conventional GDU.

The gate signals of the automatic adjusted turn-off profile are presented in Fig. 5.36. The IGBT is turned off with a reduced total gate turn-off resistance of 2.45 Ω. During this time interval, 2.2 µs < t < 3.9 µs, $R_{G,OFF2}$ is connected in parallel. As a result, the dv_{CE}/dt is increased. In the time interval 3.9 µs < t < 4.2 µs, $R_{G,OFF2}$ is disconnected, which means that the total gate turn-off resistance is increased from 2.45 Ω to 3.95 Ω. Thus the di_C/dt is adjusted in order to limit the over-voltage peak of v_{CE}. After t = 3.9 µs, $R_{G,OFF2}$ is connected again and v_{GE} remains at -15 V.

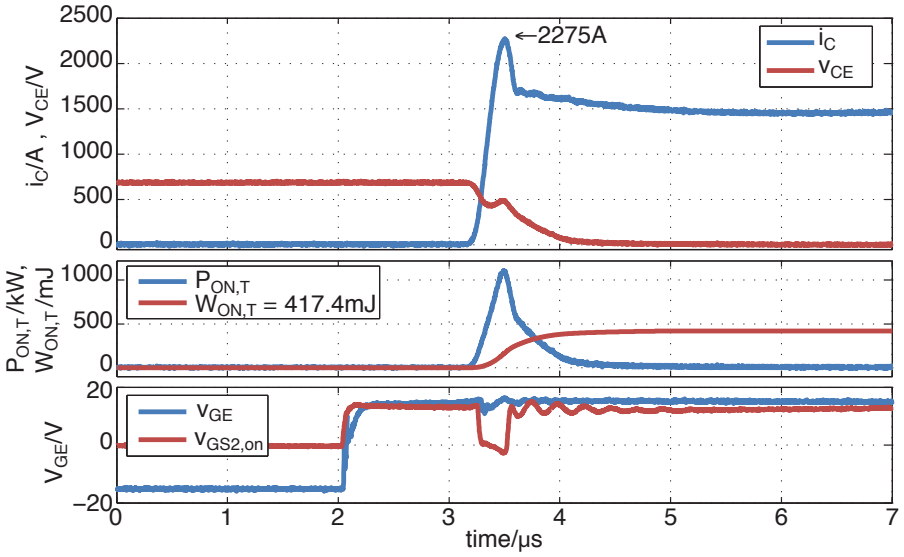


Figure 5.34: Waveforms for automatic activation of the total $R_{G,ON}$ reduction during the IGBT turn-on transient (V_{CC} = 700 V, I_C = 1400 A, T_j = 125 °C).

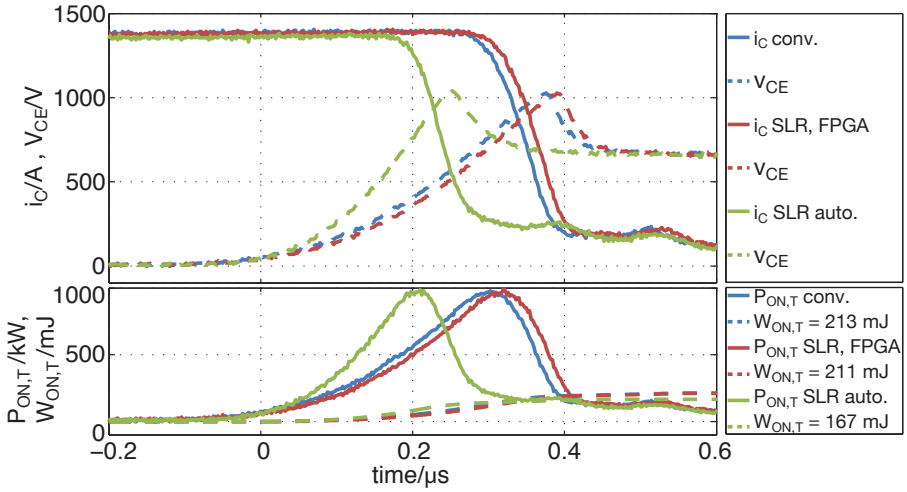


Figure 5.35: Collector current and energy losses during the turn-off transient of the IGBT with an optimal switching profile (V_{CC} = 650 V, I_C = 1400 A, T_j = 25 °C).

Fig. 5.37 shows the switching losses of the IGBT ($W_{ON,T}$ and $W_{OFF,T}$), the turn-off losses of the diode ($W_{OFF,D}$) and the total switching losses $W_{TOT} = W_{ON,T} + W_{OFF,T} + W_{OFF,D}$ at different collector current I_C values, when a conventional GDU and a GDU with the SLR scheme is used.

If a GDU with the SLR scheme is used, the IGBT turn-on losses $W_{ON,T}$ and turn-off losses $W_{OFF,T}$ are reduced in the entire current range; for example $W_{ON,T}$ is reduced by approximately 19% and $W_{OFF,T}$ is reduced by around 12% at I_C = 1400 A compared to the turn-on and turn-off losses with a conventional GDU. However, the diode turn-off losses $W_{OFF,D}$ are increases at high collector currents $I_C > 600$ A. When the collector current is I_C = 1400 A, the $W_{OFF,D}$ is increased by around 12%. The total switching losses W_{TOT} are reduced by about 12% at nominal collector current I_{CN} = 1400 A compared to the results obtained with a conventional GDU.

The new scheme, as demonstrated by the experimental results presented here, is able to recognize the switching phases in which the collector current changes and to modify the gate current by connecting gate resistances in parallel. The switching loss reduction compared to conventional operation strongly depends on the internal gate resistance value of the IGBT. An increased ratio

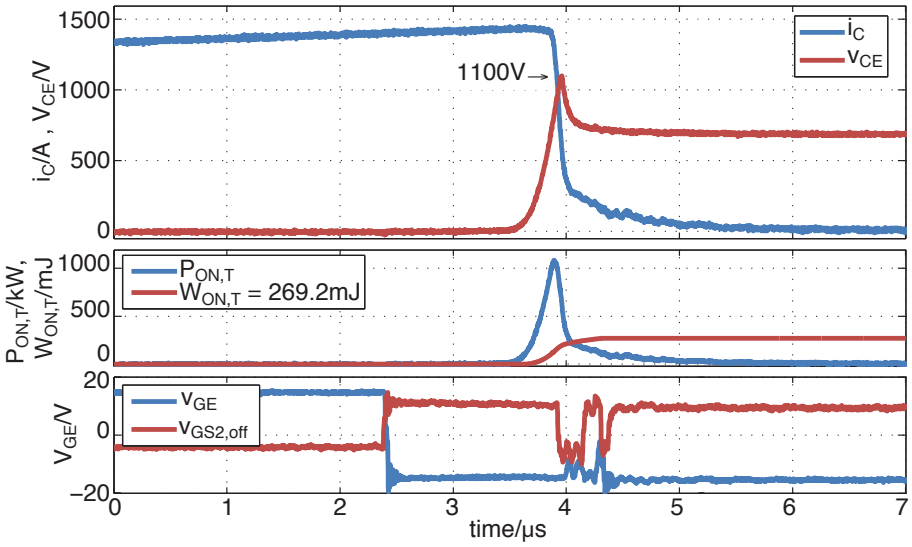


Figure 5.36: Automatic activation of the reduced $R_{G,OFF}$ during the IGBT turn-off transient (V_{CC} = 700 V, I_C = 1400 A, T_j = 125 °C).

of the external gate resistances $R_{G,ON1}$ and $R_{G,OFF1}$ to the IGBT internal gate resistance $R_{G,int}$ and an increased ratio of $R_{G,ON1}/R_{G,ON2}$ and $R_{G,OFF1}/R_{G,OFF2}$ increases the benefit of the proposed scheme. Alternatively, the GDU could operate with fixed gate resistance values and vary the gate-emitter voltage according to the switching phases.

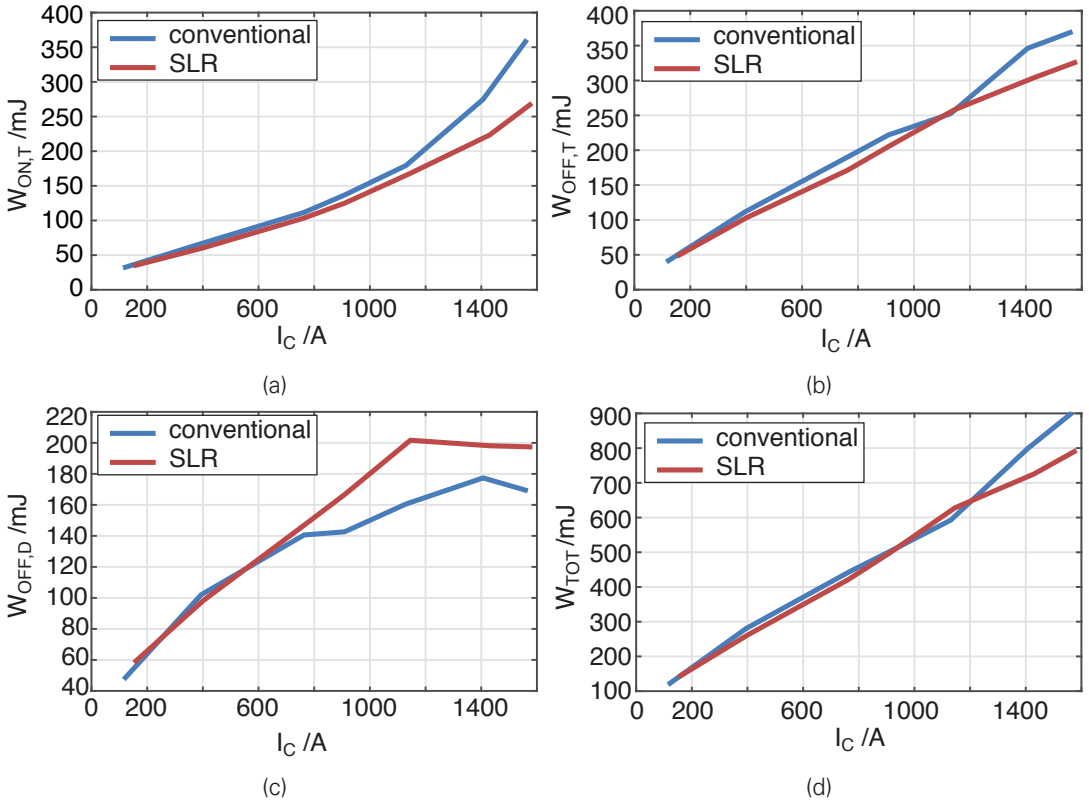


Figure 5.37: Comparison of the switching losses of the IGBT and diode at different collector currents with a GDU with the SLR scheme and a conventional GDU (V_{CC} = 700 V, T_j = 125 °C). (a) $W_{ON,T}$ = f(i_C), (b) $W_{OFF,T}$ = f(i_C), (c) $W_{OFF,D}$ = f(i_C) and (d) W_{TOT} = $W_{ON,T}$ + $W_{OFF,T}$ + $W_{OFF,D}$.

5.4 INVESTIGATION OF IGBTS WITH HIGHER GATE-EMITTER VOLTAGE

Driving IGBTs with high turn-on gate-emitter voltage V_{GEon} provides advantages in terms of loss reduction. Fig. 5.38 shows an example of a typical IGBT output characteristic. Increasing v_{GE} results in a reduction of the collector-emitter saturation voltage $V_{CE,sat}$ and, consequently, a reduction of the on-state losses.

IGBT manufacturers specify the gate-emitter voltage of the device in a range of $-20\,V < v_{GE} < 20\,V$. A high turn-on gate-emitter voltage V_{GEon} accelerates the degradation of the gate oxide, which affects the lifetime of the IGBT [82, 83]. However, in principle the turn-on gate-emitter voltage V_{GEon} can be increased far beyond the given limit ($V_{GEon} \gg 20\,V$) without immediately destroying the isolation, as the isolation capability and the width of the gate oxide define this boundary of V_{GEon} [16]. Fig. 5.39 shows a cross section of a trench cell of the (75 A / 1200 V) IGBT IGV70T120T6RM, where the gate-oxide thickness is 90 nm [84]. Regarding the isolation capability, the maximal V_{GEon} is:

$$V_{GEon,max} = 90\text{nm} \cdot 8\frac{MV}{cm} = 72\,V, \tag{5.3}$$

where $8\frac{MV}{cm}$ is the isolation capability of the gate oxide [85].

IGBTs are designed to endure a short circuit for no longer than 10 µs at a turn-on gate-emitter voltage of V_{GEon} = 15 V. In this case short circuits can be detected and turned off using conventional protection schemes like e.g. $V_{CE,sat}$ observation and soft turn-off. The saturation of the collector current $I_{C,sat}$ depends on v_{GE} according to (2.1).

To overcome the problem of a high $I_{C,sat}$ during a short circuit caused by the increased gate-emitter voltage, as indicated by (2.1), the *fast short circuit protection method*, presented in Section 5.2, is used.

In this section, the influence of a high gate-emitter voltage on the losses of the IGBT is investigated. Moreover, a GDU concept with a short circuit protection scheme for IGBTs with a turn-on gate-emitter voltage of V_{GEon} = 35 V is proposed.

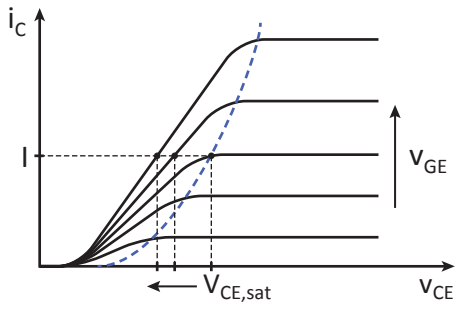


Figure 5.38: An example output characteristic of an IGBT.

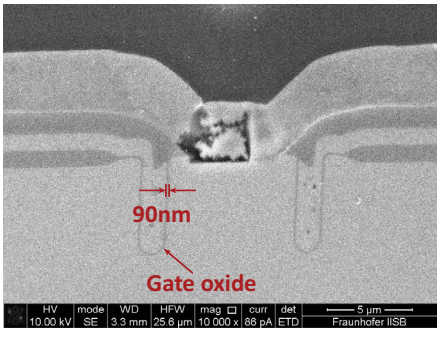


Figure 5.39: Picture of a cross section of a cell, indicating the gate-oxide thickness of the IGBT IGV70T120T6RM (75 A / 1200 V) [84].

5.4.1 Experimental investigation of the on-state losses

5.4.1.1 Test description

Due to the lack of suitable datasheet information or device models for the increasing V_{GEon} range being considered, the reduction of the on-state losses with high V_{GEon} was experimentally investigated. The topology and example waveforms are shown in Fig. 5.40 [86]. The topology consists of an H-bridge inverter, a transformer and a rectifier. The load contains an inductor and the IGBT which is operated in the on-state. The output current i_C is controlled by modifying the input voltage V_{CC} and the duty cycle of the modulation pulse. The turn-on gate-emitter voltage V_{GEon} is adjusted with an external power supply between 15 and 60 V.

The experimental set-up is shown in Fig. 5.41. The junction temperature T_j is monitored with the internal IGBT thermistor and an external Pt100 sensor. The test conditions are listed in Table 5.7.

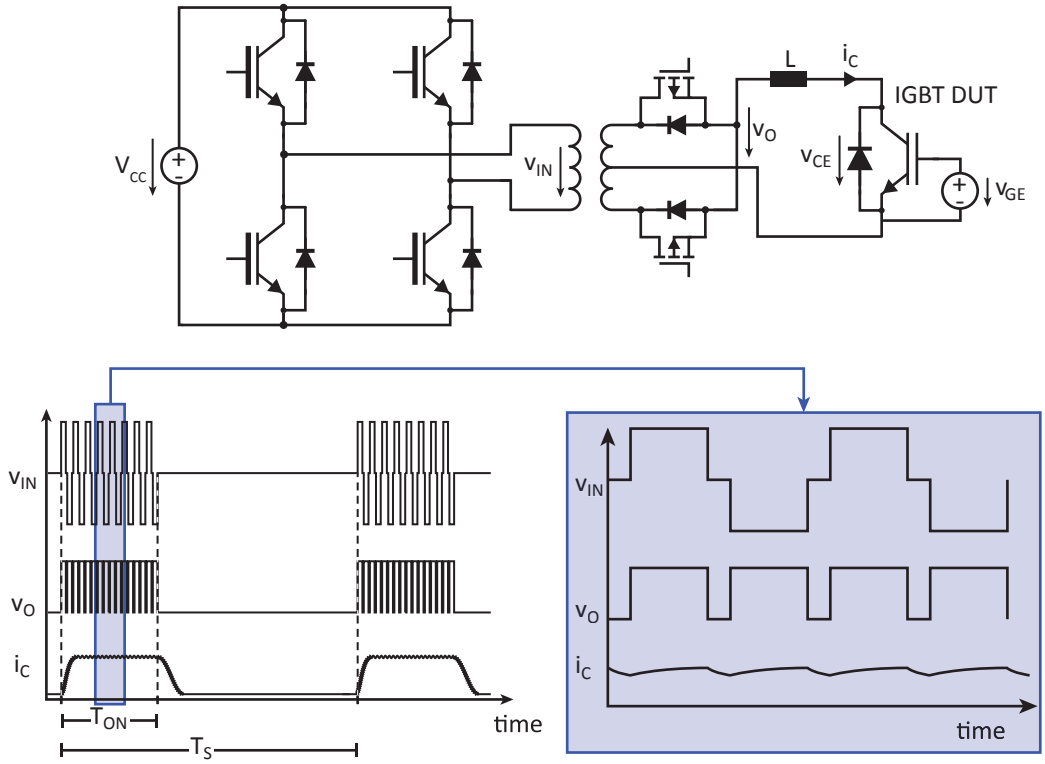


Figure 5.40: Topology of the converter used for on-state investigation and its input and output waveforms.

Table 5.7: Test conditions for the on-state loss investigations of IGBTs with high V_{GEon}

Variable	Description
IGBT	Fuji:2MBI1400VXB-170E-50, 1400 A / 1700 V
V_{CC}	50...420 V
i_C	100...2800 A
T_j	125 °C
V_{GEon}	15...60 V in steps of 5 V

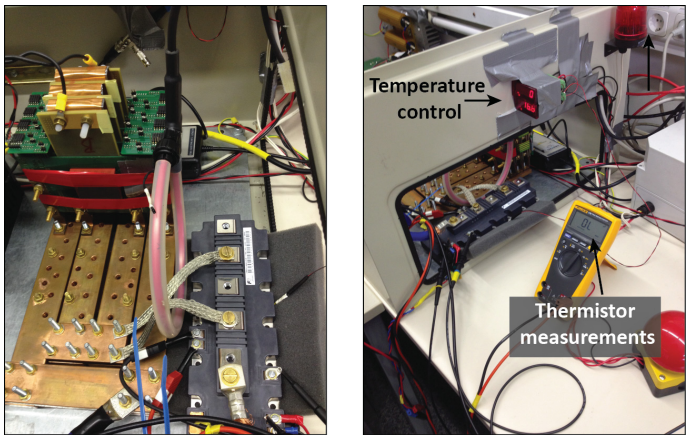


Figure 5.41: Photographs of the laboratory set-up for on-state voltage investigation with increased v_{GE}.

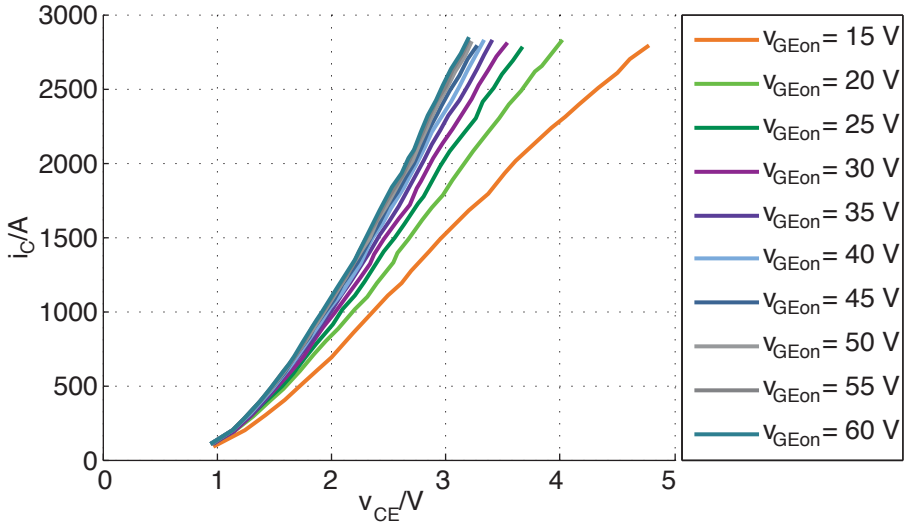


Figure 5.42: Output characteristic at different gate-emitter voltages (I_C = 1400 A, T_j = 125°C).

5.4.1.2 Experimental results

The output characteristic $i_C = f(v_{CE})$ of the IGBT at different V_{GEon} is presented in Fig. 5.42. At nominal current I_{CN} = 1400 A, the collector-emitter voltage v_{CE} is reduced by 18.2% if V_{GEon} = 35 V and by 21.6% if V_{GEon} = 60 V, compared to v_{CE} at V_{GEon} = 15 V. Fig. 5.43 shows the collector-emitter voltage as a function of the turn-on gate-emitter voltage $v_{CE} = f(V_{GEon})$ at nominal collector current I_{CN} = 1400 A. The results are also listed in Table 5.8. It is shown that a turn-on gate-emitter voltage V_{GEon} increased beyond 35 V ($V_{GEon} > 35$ V) does not provide a significant reduction of $V_{CE,sat}$ and increases the risk of destruction of the IGBT in case of short circuits.

5.4.2 Experimental investigation of switching losses

To investigate the influence of a high turn-on gate-emitter voltage V_{GEon} on the switching losses, a GDU was designed and built. The implementation is shown in Fig. 5.44. A maximal turn-on gate-emitter voltage of V_{GEon} = 35 V was selected. A bootstrap driver with independent turn-on and turn-off signals (s_1 and s_2) was used to control the output stage. Moreover, a DC-DC converter power supply controlled with an FPGA through the signal *ctrl* generates a variable output voltage

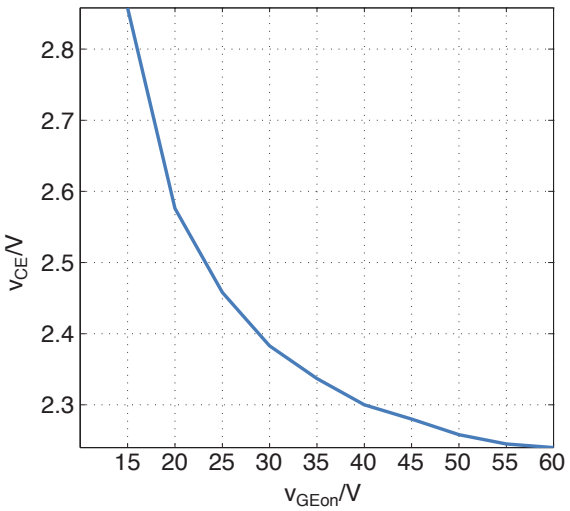


Figure 5.43: Collector-emitter voltage at different gate-emitter voltages (I_C = 1400 A, T_j = 125°C).

Table 5.8: Collector emitter voltage at different turn-on gate-emitter voltages. I_C = 1400 A, T_j = 125°C

V_{GEon}	v_{CE}	$\frac{(v_{CE}-v_{CE,15})}{v_{CE,15}}$ %
15 V	2.858 V	0%
20 V	2.576 V	9.8%
25 V	2.458 V	14.0%
30 V	2.383 V	16.6%
35 V	2.337 V	18.2%
40 V	2.30 V	19.5%
45 V	2.280 V	20.2%
50 V	2.258 V	20.9%
55 V	2.245 V	21.4%
60 V	2.240 V	21.6%

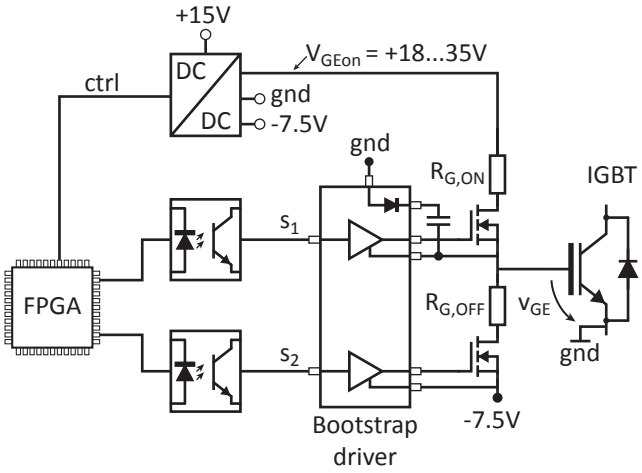


Figure 5.44: Block diagram of the output stage of the GDU prototype for switching with high v_{GE}.

from 18 to 35 V. However, the tests are carried out at two turn-on gate-emitter voltages V_{GEon} = 18 V and V_{GEon} = 35 V.

5.4.2.1 Test description

The experimental results were obtained in a buck converter, as shown in Fig. 5.45. Three different conditions were tested:

Test condition (a): The parameters are set inside the recommended range of the IGBT specifications (V_{GEon} = 18 V < 20,V).

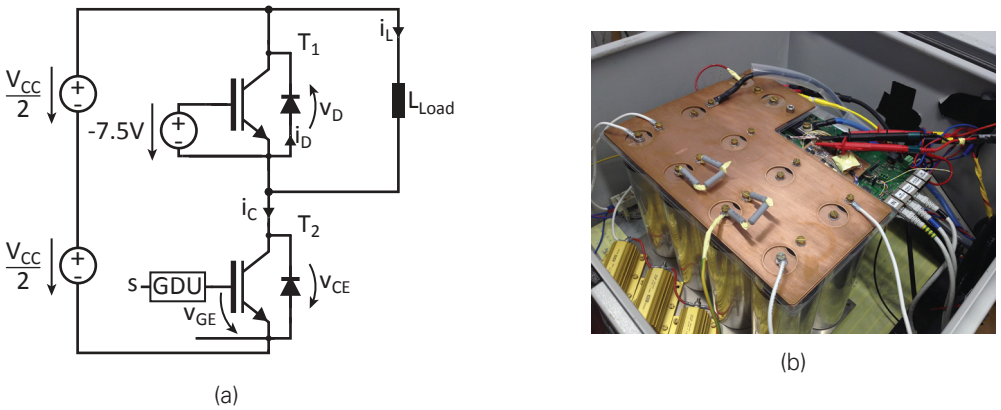
Test condition (b): V_{GEon} = 35 V and same di_C/dt as in test condition (a) during the turn-on transient. $R_{G,ON}$ for condition (b) > $R_{G,ON}$ for condition (a).

Test condition (c): V_{GEon} = 35 V and higher di_C/dt as test condition (a) during the turn-on transient. $R_{G,ON}$ for condition (c) is equal to the $R_{G,ON}$ for condition (a).

The test conditions and parameters are summarized in Table 5.9

Table 5.9: Test conditions for the switching losses investigations of IGBTs

Variable	Description
IGBT	Fuji:2MBI1400VXB-170E-50, 1400 A / 1700 V
V_{CC}	700 V
i_C	150...1400 A
L_{Load}	25.3 μH
C_1	2.8 mF
T_j	25 and 125 °C
Condition (a)	V_{GEon} = +18 V, V_{GEoff} = −7.5 V; $R_{G,ON}$ = 0.55 Ω; $R_{G,OFF}$ = 1.4 Ω.
Condition (b)	V_{GEon} = +35 V, V_{GEoff} = −7.5 V; $R_{G,ON}$ = 5.5 Ω; $R_{G,OFF}$ = 1.4 Ω.
Condition (c)	V_{GEon} = +35 V, V_{GEoff} = −7.5 V; $R_{G,ON}$ = 0.55 Ω; $R_{G,OFF}$ = 1.4 Ω.



(a)

(b)

Figure 5.45: Set-up used for switching loss investigation. (a) circuit topology, and (b) photograph of the experimental set-up.

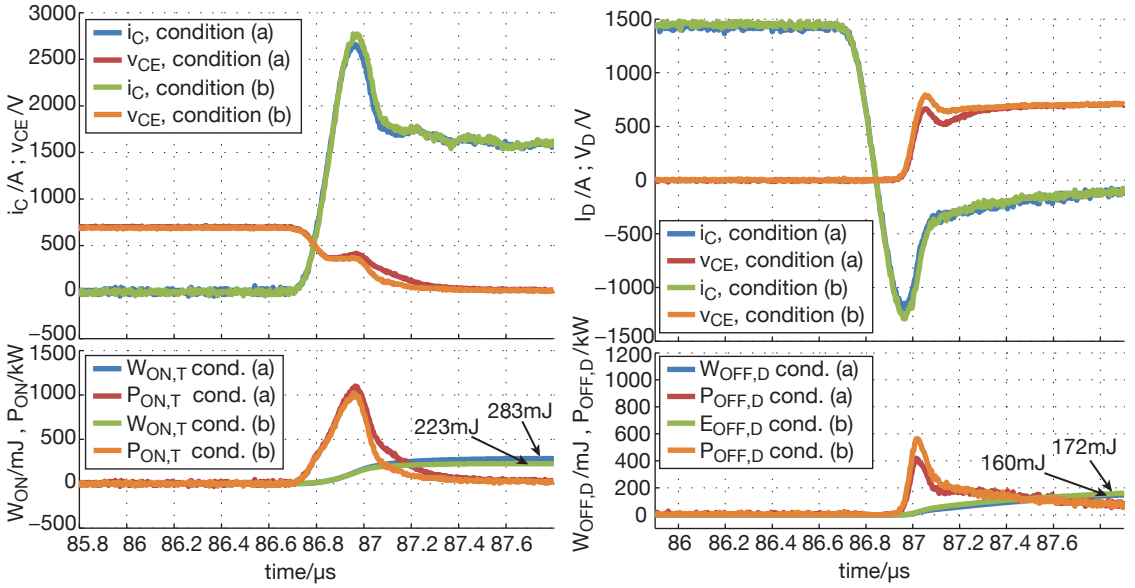


Figure 5.46: Collector current and switching losses during the turn-on transient with same $\frac{di_C}{dt}$ (V_{CC} = 700 V, I_C = 1400 A, T_j = 125°C and V_{GEon} = 18 and 35 V). (a) IGBT turn-on transient, and (b) diode turn-off transient.

5.4.2.2 Experimental results

Fig. 5.46 shows the turn-on transient of the IGBT for conditions (a) and (b). When the turn-on gate-emitter voltage is V_{GEon} = 35 V, v_{CE} reaches $V_{CE,sat}$ 120 ns faster compared to condition (a). As a consequence, the IGBT turn-on losses $W_{ON,T}$ are reduced by approximately 20% and the diode turn-off losses $W_{OFF,D}$ (Fig. 5.46b) are increased by around 7.5 %.

Fig. 5.47 shows the turn-on transient of the IGBT for conditions (a) and (c). With a high di_C/dt, v_{CE} decreases 250 ns faster than with a standard di_C/dt (a). The IGBT turn-on losses $W_{ON,T}$ are reduced by approximately 65% and the diode turn-off losses $W_{OFF,D}$ (Fig. 5.47b) are increased by approximately 30%. The peak collector current of the IGBT and the peak reverse recovery current of the diode are distinctly increased at the high di_C/dt. The safe operating area of the IGBT and diode must be considered in the selection of the gate current of the switching profile (e.g. $R_{G,ON}$).

The IGBT turn-off transients for condition (a) and (b) are presented in Fig. 5.48. In both situations the IGBT is turned off with V_{GEoff} = −7.5 V and a gate turn-off resistance $R_{G,OFF}$ = 1.4 Ω, which is also applied in condition (c). Therefore v_{CE}, i_C and the IGBT turn-off losses $W_{OFF,T}$ are similar. However, the turn-off delay of the IGBT increases by approximately 1 µs when the turn-on gate-emitter voltage is V_{GEon} = 35 V.

The total switching losses W_{TOT}, are presented in Fig. 5.49.Compared to condition (a), for condition (b) the total switching losses at nominal current are reduced by 9% (red line) and for condition (c) by 18%.

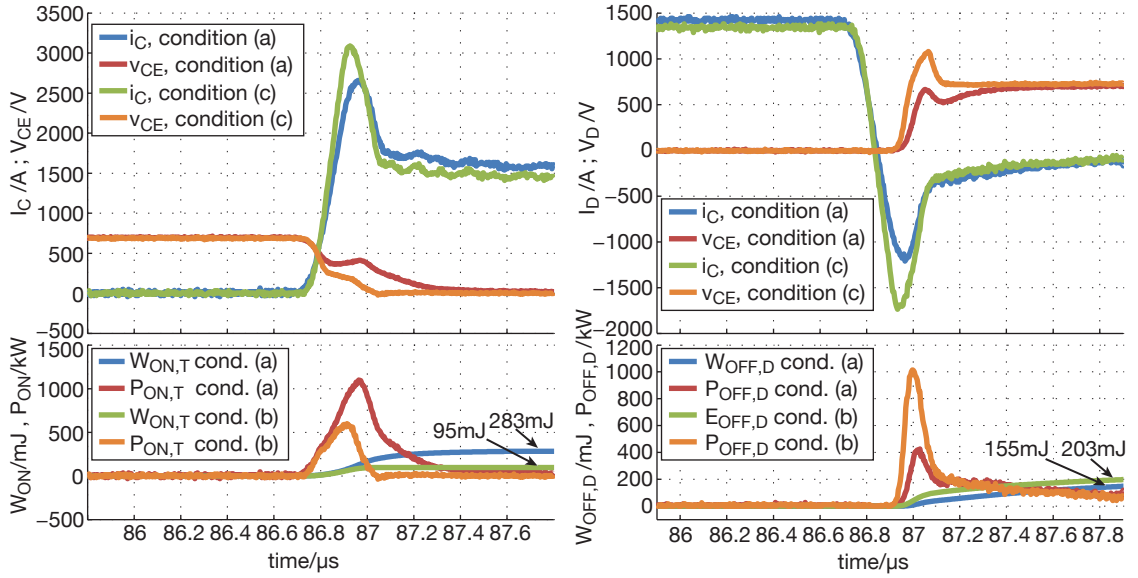


Figure 5.47: Collector current and switching losses during the turn-on transient with similar $\frac{di_C}{dt}$ (V_{CC} = 700 V, I_C = 1400 A, T_j = 125°C and V_{GEon} = 18 and 35 V). (a) IGBT turn-on transient, and (b) Diode turn-off transient.

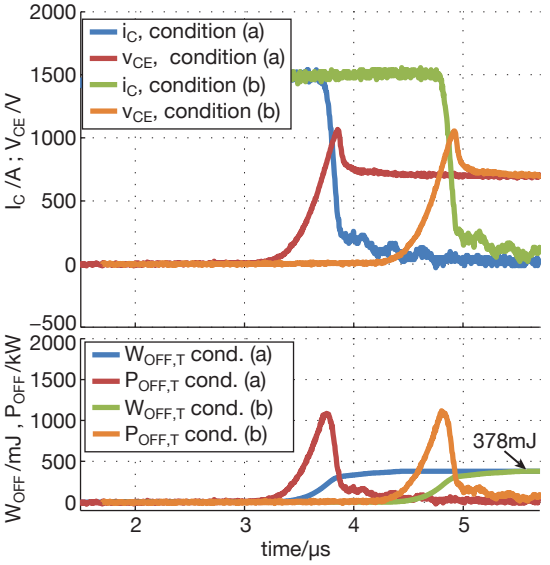


Figure 5.48: IGBT turn-off transient with different V_{GEon} (V_{CC} = 700 V, I_C = 1400 A, T_j = 125 °C and V_{GEon} = 18 and 35 V).

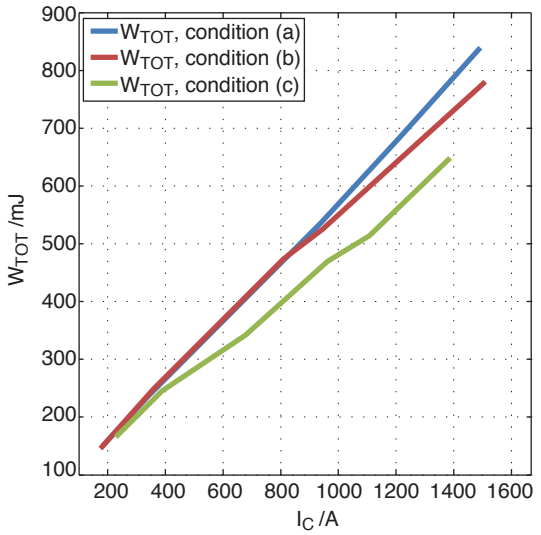


Figure 5.49: Total switching losses of the IGBT with high V_{GEon}. W_{TOT} = f(I_C) (V_{CC} = 700 V; T_j = 125 °C and V_{GEon} = 18 and 35 V).

5.4.3 Short circuit protection scheme

The IGBT is tested under short circuit conditions with a turn-on gate-emitter voltage of V_{GEon} = 35 V. The short circuit is detected with the *fast short circuit protection method* (FSCP) presented in Section 5.2, which is based on the sensed voltage v_{bond} across the internal stray inductance L_{bond} of the IGBT module.

The IGBT is turned on and off in two stages, as shown in Fig. 5.50. The IGBT is turned on

with 15 V and after a few microseconds (e.g. 2–5 µs), v_{GE} is increased to 35 V. This scheme allows a standard protection method ($V_{CE,sat}$) for the device in case of short circuit type I. In this implementation, the gate-emitter voltage is actively modified by turning on and off the trigger signals s_1 and s_2 while the DC-DC voltage remains constant at 35 V.

During t_0–t_1 the signal s_2 is activated (=1) and s_1 is deactivated (=0), and the IGBT is the in off state with V_{GEoff} = –7.5 V. During t_1–t_2 the signal $s_1 = 1$ and $s_2 = 0$ and v_{GE} starts to increase. The IGBT is turned on. When the gate-emitter voltage is v_{GE} = 15 V, $s_1 = s_2 = 0$, the gate is floating and v_{GE} is kept at 15 V for a defined interval (e.g. 2 µs). If no short circuit type I is detected, v_{GE} is increased to 35 V by setting $s_1 = 1$ and $s_2 = 0$ (t_3–t_4).

In case of short circuit type II, the IGBT is turned off in two stages in order to reduce the short circuit current and to desaturate the IGBT quickly. In a first step, the gate-emitter voltage v_{GE} is reduced immediately after the detection of the short circuit by setting the signals $s_1 = 0$ and $s_2 = 1$ (t_4–t_5). When v_{GE} reaches a certain desired value, e.g. 15 V or 12 V, the digital signals s_1 and s_2 are set to zero and v_{GE} is kept constant for a certain time. Therefore, the short circuit current is reduced and the IGBT is desaturated. Thereafter, the trigger signals are set as $s_1 = 0$ and $s_2 = 1$ and the IGBT is completely turned off ($t > t_6$).

It should be mentioned that the chosen implementation in Fig. 5.50 has the disadvantage that the gate is floating (high impedance connection to the GDU supply voltages). Under short circuit conditions this realization can be disadvantageous if it is not combined with an effective clamping of the gate-emitter voltage. An alternative realization would be a GDU with three supply voltages (e.g. V_{GEon1} = +15 V, V_{GEon2} = +35 V and V_{GEoff} = –7.5 V) and a corresponding three voltage level output stage.

5.4.3.1 Experimental verification

Test description

The short circuit II protection scheme is tested in a buck converter, as shown in Fig. 5.45. The short circuit is produced by triggering the upper IGBT T_1 while the lower IGBT T_2 is in the on-state. The test conditions are listed in Table 5.10.

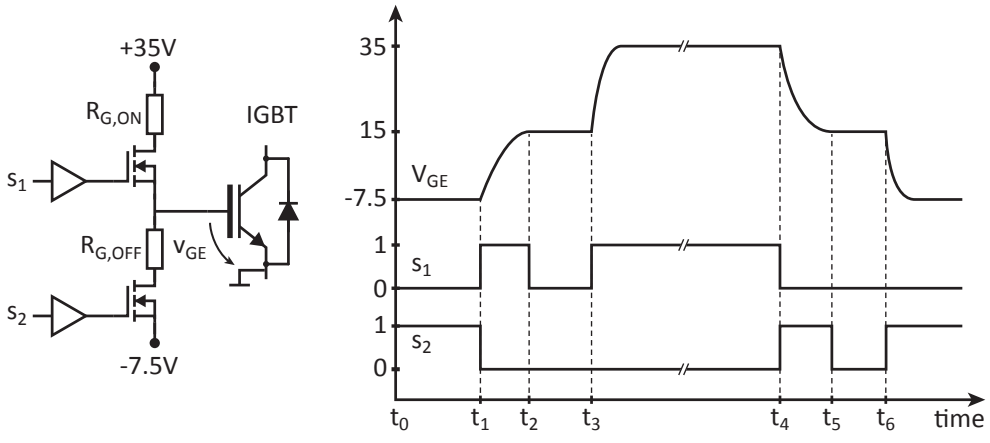


Figure 5.50: Example of the two-stage gate-emitter voltage driving strategy.

Table 5.10: Test conditions for the short circuit investigations of IGBTs with high v_{GE}

Variable	Description
IGBT	Fuji:2MBI1400VXB-170E-50, 1400 A / 1700 V
V_{CC}	50...500 V
i_C	1400 A
T_j	125 °C
v_{GE}	35 V

Experimental results

Experimental results are shown in Figs. 5.51 and 5.52. The collector current i_C, the collector emitter voltage v_{CE}, the gate-emitter voltage v_{GE} and short circuit detection signal $v_{meas,i\text{-}on}$ are shown. During the short circuit test, i_C reaches 7 kA. When v_{GE} is reduced to 15 V (Fig. 5.51), i_C is reduced to 4 kA. However, i_C starts to rise again because the gate is floating and, due to the Miller effect, the gate-emitter capacitance C_{GE} is charged, which, in turn, increases the value of v_{GE}. By reducing v_{GE} to 12.5 V (Fig. 5.52), i_C can be reduced to 2 kA. In that case the IGBT is already saturated when the gate is left open ($s_1 = s_2 = 0$). Therefore, v_{GE} and i_C do not increase in the state of the floating gate. After 2 µs the IGBT is completely turned off.

The proposed realization can be improved by a GDU with a three level output stage with three supply voltages (e.g. $V_{GEon1} = +15$ V, $V_{GEon2} = +35$ V and $V_{GEoff} = -7.5$ V). With this configuration, the gate would not float and it would not be charged during a short circuit situation. However, the investigations show that the proposed scheme of a two stage v_{GE} turn-on transient and a two stage turn-off transient in the case of short circuit type II is an effective method to handle short circuit situations if the IGBTs are operated at increased turn-on gate-emitter voltages. The required fast short circuit detection can be realized e.g. with the *fast short circuit protection method* (FSCP) presented in Section 5.2.

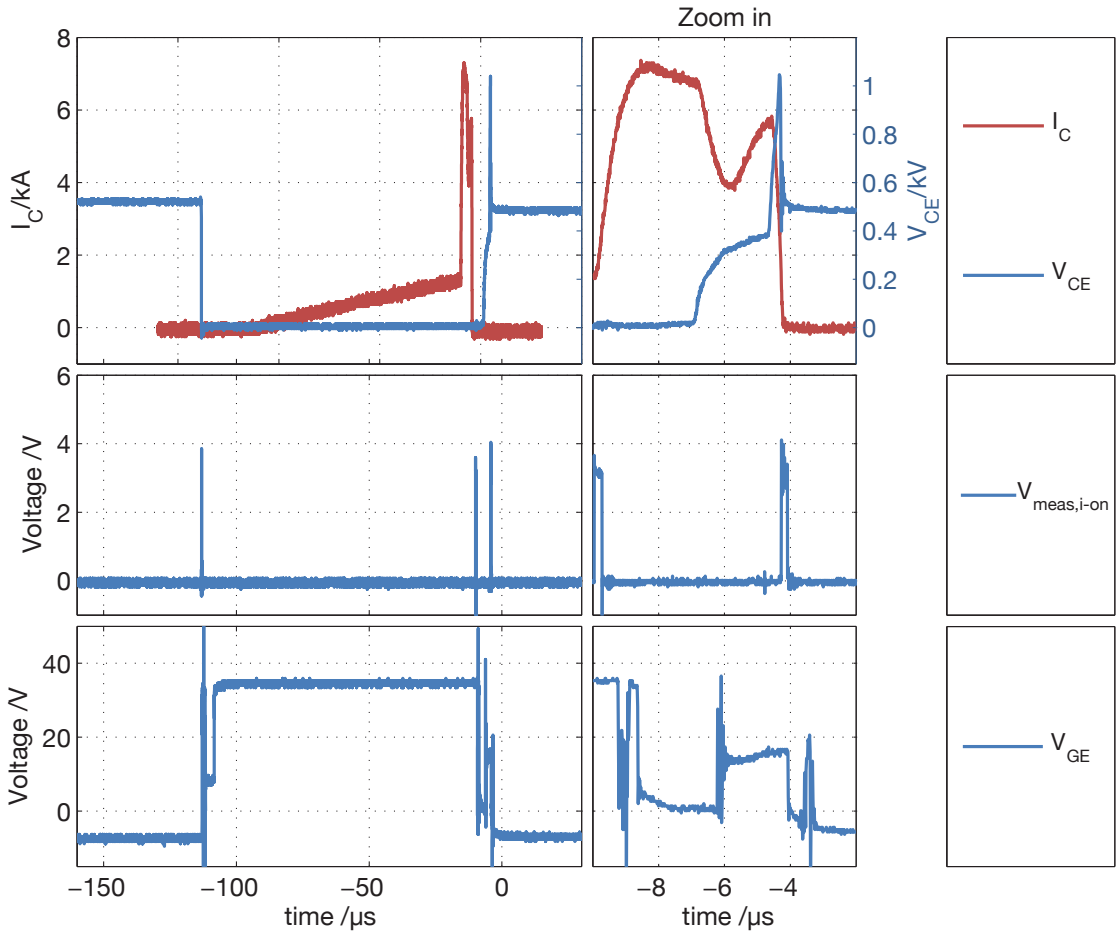


Figure 5.51: Experimental result of a short circuit type II. v_{GE} is reduced from v_{GE} = 35 V to v_{GE} = 15 V (V_{CC} = 500 V, I_C = 1400 A, T_j = 125 °C).

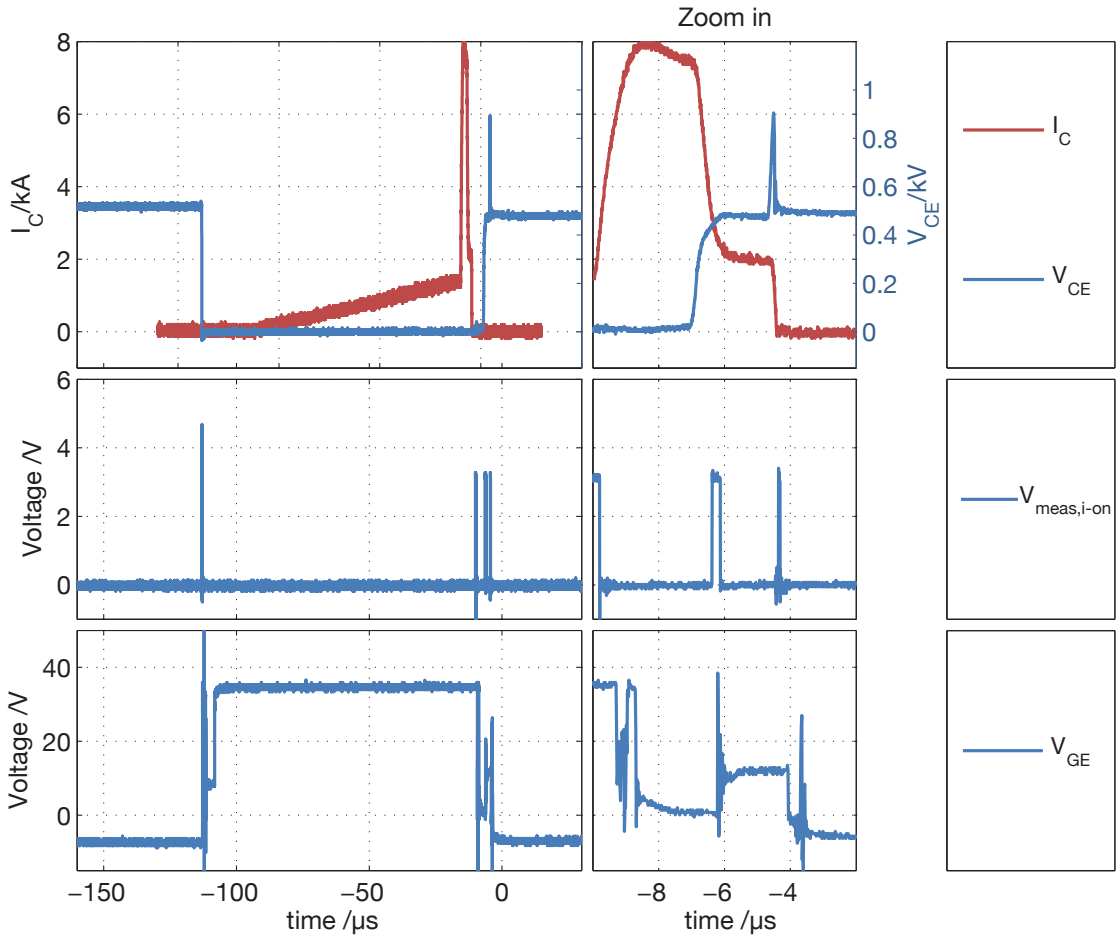


Figure 5.52: Experimental result of a short circuit type II. v_{GE} is reduced from v_{GE} = 35 V to v_{GE} = 12.5 V (V_{CC} = 500 V, i_C = 1400 A, T_j = 125 °C).

5.5 SUMMARY

In this chapter, four new concepts for GDU functions were presented which use the measurement of the voltage across the stray inductance L_{bond} of the IGBT.

The first section presents a new method for static balancing of the collector current. Experimental results were obtained with two IGBT modules connected in parallel. The stationary imbalance of collector currents was reduced from 25% to 5%.

The second section describes a fast short circuit protection method (FSCP) for IGBT modules. With this, the IGBT, for instance, can be turned off in a short circuit situation in less than 1µs, which is 10 times faster than with the standard $V_{CE,sat}$ detection method. Moreover, v_{GE} can be reduced after the detection of the short circuit. Thus, the junction temperature T_j of the device can be reduced by more than 50% compared to the standard method.

Furthermore, the new method can also distinguish a short circuit type I from type II and applies different actions according to the type of short circuit. It is noteworthy that the new method is simple and inexpensive to implement, which is a important advantage for industrial converters.

The third section presents a method to reduce the switching losses in an IGBT by way of an improved gate switching profile. In this method, the gate current is modified actively during the switching transient according to the switching phases. The phases are detected with the sensed voltage across the stray inductance. The total switching losses are reduced by about 12% compared to the conventional switching method.

The fourth section shows the operation of an IGBT with an increased turn-on gate-emitter voltage V_{GEon} ($V_{GEon} > 15\,V$). The on-state losses can be reduced by 18% if $V_{GEon} = 35\,V$ and by 21.5% if $V_{GEon} = 60\,V$, compared to the on-state losses if $V_{GEon} = 15\,V$. The total switching losses are reduced by 9% if $V_{GEon} = 35\,V$ compared to $V_{GEon} = 15\,V$, assuming similar di_C/dt in both situations.

Additionally, the scheme has been tested during short circuit situations, where the IGBT is turned off in two steps after the detection of the failure, providing for safe operation of the device. All these new concepts have been implemented with simple and inexpensive electronic circuitry, which is an important advantage for possible industrial implementations.

6 CONCLUSIONS

In this work new concepts for gate drive units (GDUs) for IGBTs and RC-IGBTs were presented. They were designed and implemented with simple and inexpensive electronic circuitry, which is an important advantage for possible industrial applications.

A GDU scheme with two novel methods to estimate the collector current through the IGBT module based on the measurement of the voltage across the IGBT internal stray inductance were presented. Assuming a prior calibration, these methods are independent of the value of the IGBT parameters such as stray inductance, gate resistances, gate-emitter threshold voltage and tolerances of electronic components. The calibration process and the estimation of the collector current were implemented in an FPGA algorithm. The experimental results show a current estimation error lower than 8% for collector currents higher than 150 A for the (650 A / 1700 V) IGBT module under consideration.

A scheme to statically balance the collector currents of parallel connected IGBTs was derived, designed and implemented in another GDU concept. The current balancing is achieved by active variation of the gate-emitter voltage according to the estimated collector current value. The experimental results of the proposed scheme showed a fast reduction of the static current imbalance from 25% to 5%.

A new fast short circuit protection method (FSCP) for IGBT modules was derived, designed and implemented in another GDU. This concept allows different turn-off procedures of the IGBT after the detection of the short circuit, according to the type of short circuit (short circuit type I and type II). The experimental results showed that the considered IGBT could be turned off in less than 1 µs, which means 10 times faster than with the standard $V_{CE,sat}$ detection method. Furthermore, by reducing the gate-emitter voltage v_{GE}, the collector current was reduced during the short circuit. As a consequence the rise of the IGBT junction temperature T_j was decreased by more than 50%. This method enables a simple and inexpensive implementation, which is an important advantage for a possible industrial implementation.

Another scheme implemented in a GDU features an improved gate switching profile of the IGBT in order to reduce the switching losses. In this method, the gate current is actively modified during the switching transients according to the switching phases. These phases are detected with the sensed voltage across the stray inductance. The experimental results showed that the switching losses can be reduced by 25% compared to the standard switching method for the (1400 A / 1700 V) IGBT module being considered.

In order to reduce the conduction losses, a GDU with an increased turn-on gate-emitter voltage ($V_{GEon} > 20$ V) were investigated. The on-state losses are reduced by 18% if $V_{GEon} = 35$ V and by

21.5% if V_{GEon} = 60 V, compared to the on-state losses if V_{GEon} = 15 V. The total switching losses $W_{TOT} = W_{ON} + W_{OFF} + W_{OFF,D}$, were reduced by 9% if V_{GEon} = 35 V compared to the total switching losses W_{TOT} if V_{GEon} = 15 V, assuming similar di_C/dt in both situations. Besides, the scheme was tested during short circuit situations of the IGBT. An increase of v_{GE} also increases the collector current i_C during a short circuit. In the new concept the short circuit is rapidly detected with the FSCP method and the gate-emitter voltage v_{GE} is reduced e.g. to 15 V or 12 V in a first step until the IGBT is desaturated and then the IGBT is turned off, providing safe operation of the semiconductor device.

The switching behaviour of a new (200 A / 1200 V) reverse conducting IGBT (RC-IGBT) was investigated. Moreover, a new trigger pulse pattern to drive the RC-IGBT was derived, designed and implemented. The experimental results showed that the switching losses were reduced by 35% in the IGBT and by 60% in the RC-IGBT compared to the switching losses when a RC-IGBT without gate control in diode mode is used. Compared with a standard diode, the investigated RC-IGBT had 20% lower turn-off losses, which also reduces the turn-on losses of an IGBT by 25%.

The proposed gate pulse pattern can be automatically adapted to the RC-IGBT parameters by a simple double pulse test, implemented in an FPGA. The algorithm modifies the pulse pattern according to the variation of the reverse recovery current, which is estimated with the sensed voltage across the RC-IGBT stray inductance. Furthermore, the proposed pulse pattern scheme also includes a strategy to avoid possible short circuits.

A three phase 2L-VSC converter with RC-IGBTs was simulated, where RC-IGBTs were used instead of diodes. The results showed a reduction of 3.2% of the total losses for a power factor of 1. The RC-IGBT showed a good performance and it could be an interesting alternative to a IGBT-diode configuration. However, this semiconductor device requires additional expense for the GDU (hardware and software) to generate the derived pulse pattern.

All these new GDU concepts have been implemented with simple and inexpensive electronic circuitry, which is an important feature for a possible industrial implementations. During the completion of this dissertation work, two papers [1, 2] were published and three patents [3–5] were filed.

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